

GA-M51GM-S2G

SHEET TITLE

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05	PROCESSOR DDR2 INTERFACE
06	PROCESSOR DDR2 INTERFACE
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13	C51 PCI-EXPRESS
14	C51 RGB
15	C51 PWR/GND
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21	MCP51 PWR/GND
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24	PCI 1,2,SLOT
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SHEET TITLE Revision:1.0

26	AUDIO JACK, L_OUT, F_AUDIO
27	H/W MONITOR & FAN CONTROL
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29	PWM ISL6566
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31	POWER SEQUENCE
32	DDRII POWER
33	BIOS ATX POWER CONNCTOR
34	COMA,B, LPT PORT
35	FRONT PANEL
36	ITE 8716GB/CX
37	Marvell 88E1116
38	TI TSB43AB23 1394a

Model Name:GA-M51GM-S2G

Component value change history

Version: 1.0

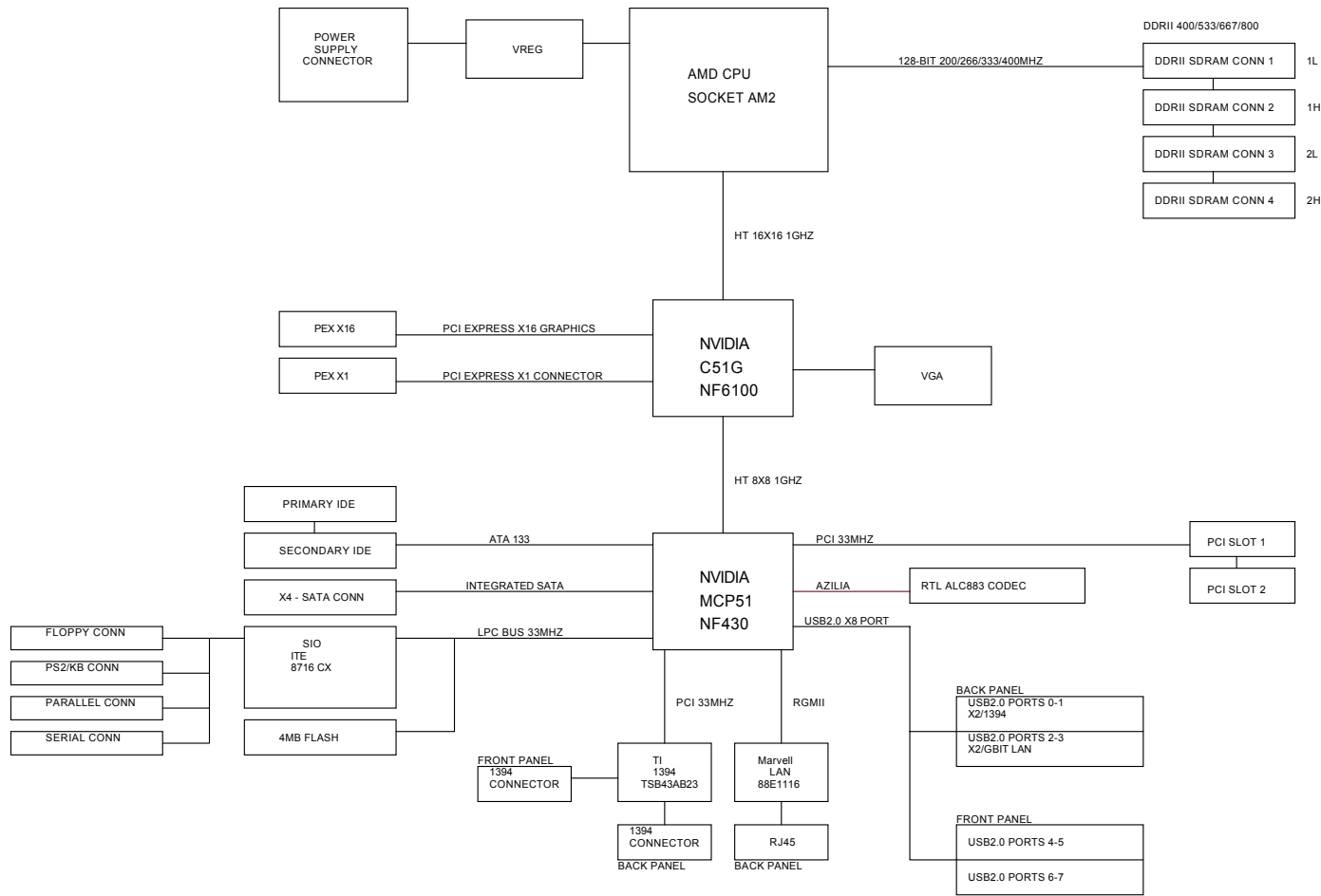
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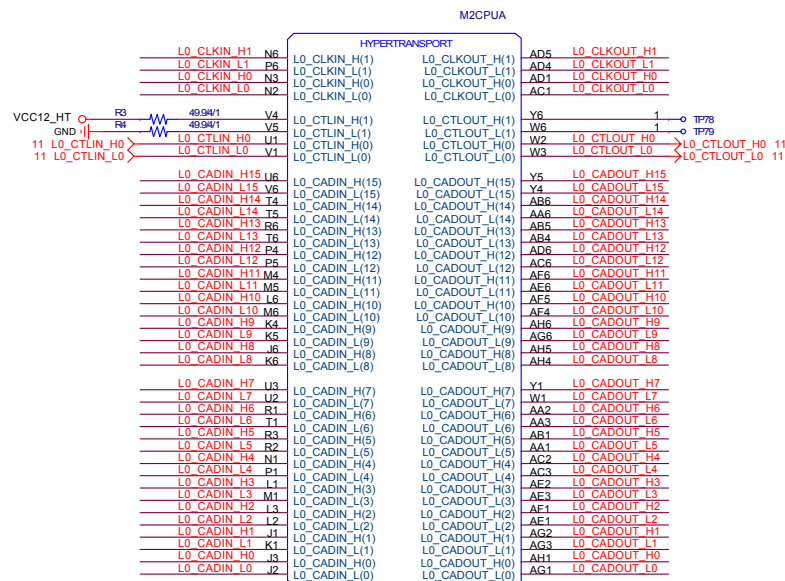
Circuit or PCB layout change for next version

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BLOCK DIAGRAM



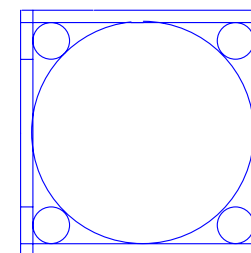
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L0_CADIN_H[0..15] L0_CADIN_L[0..15] 11
L0_CLKIN_L[0..1] L0_CLKIN_H[0..1] 11
L0_CLKIN_H[0..1] L0_CLKIN_L[0..1] 11
L0_CADOUT_L[0..15] L0_CADOUT_H[0..15] 11
L0_CADOUT_H[0..15] L0_CADOUT_L[0..15] 11
L0_CLKOUT_L[0..1] L0_CLKOUT_H[0..1] 11
L0_CLKOUT_H[0..1] L0_CLKOUT_L[0..1] 11



CPU_VDD_RUN = VCORE
CPU_VDDA_RUN = VDDA25
VLDT_RUN = VCC12_HT
CPU_VDDIO_SUS = DDR18V
CPU_VTT_SUS = DDRVTT

VLDT_A = VCC12_HT
VLDT_B = HT12B

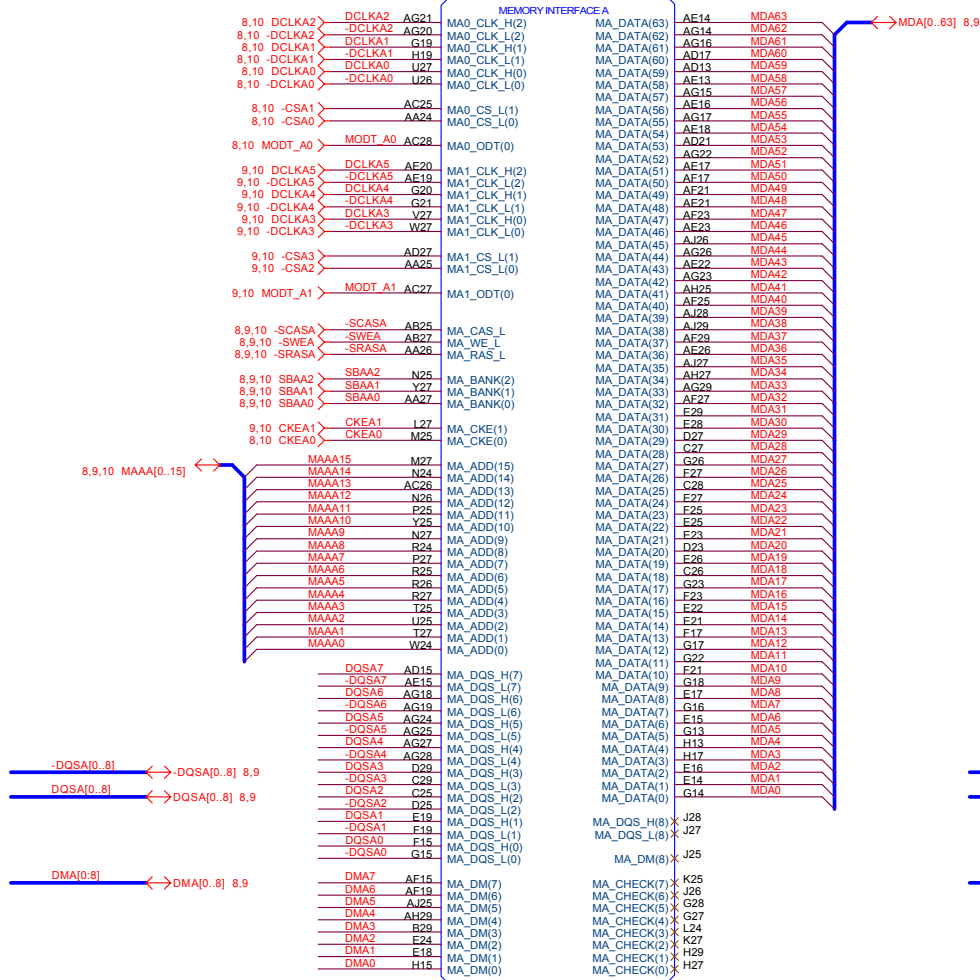
SOCKET_M2
M2/[12KRC-04K807-21R]



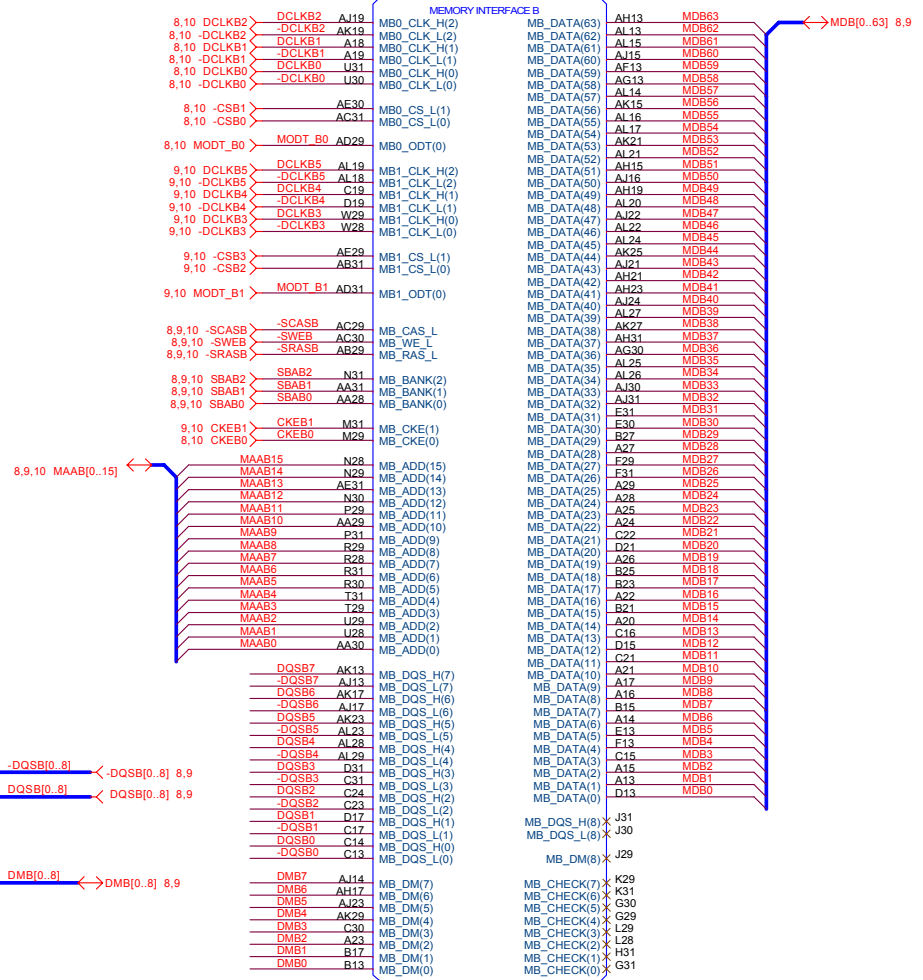
GIGABYTE

Title			
CPU HYPER TRANSPORT			
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M2CPUB

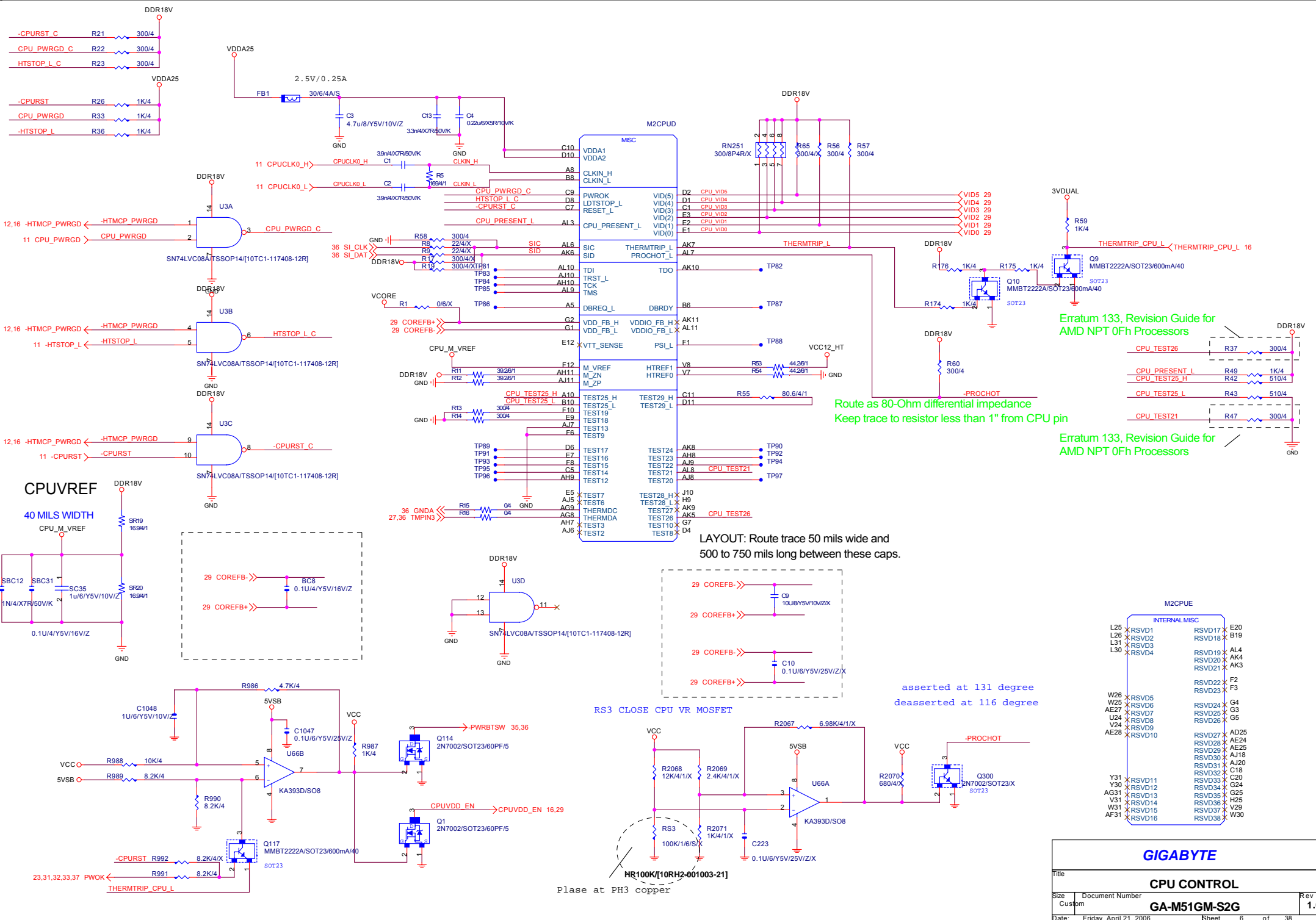


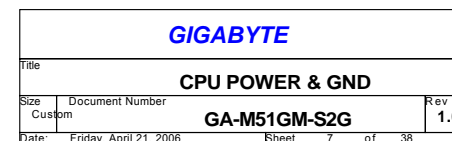
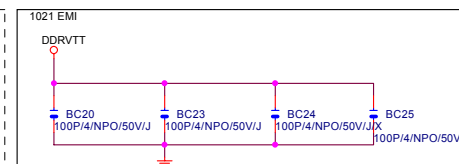
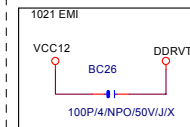
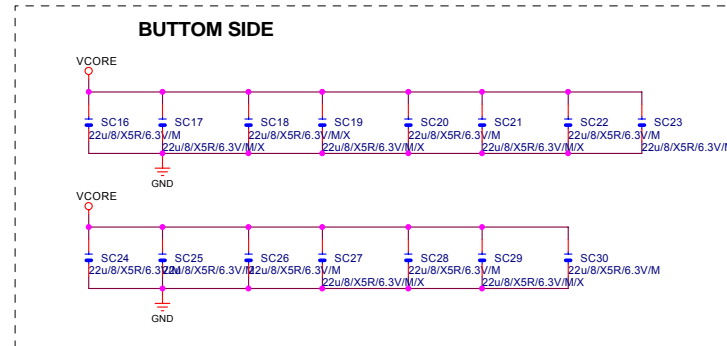
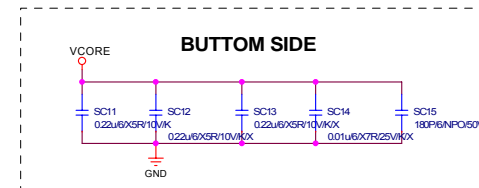
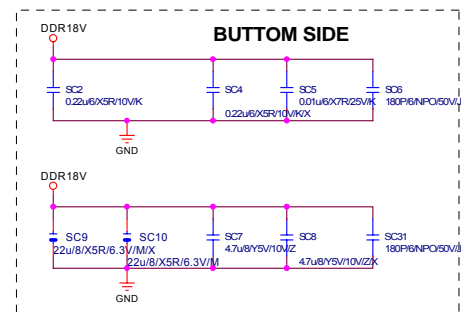
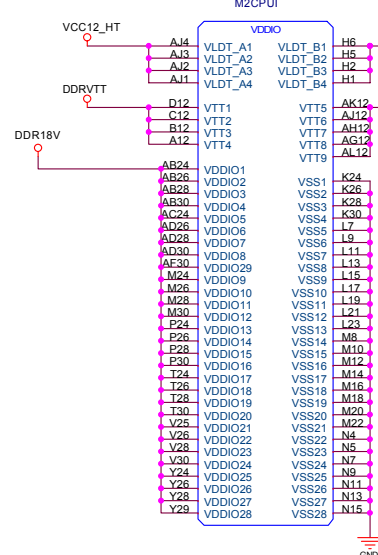
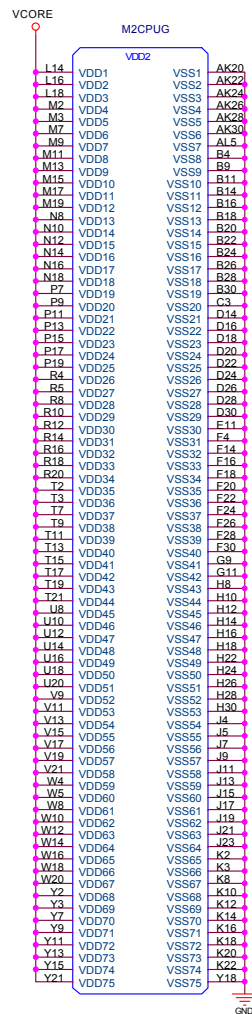
M2CPUC



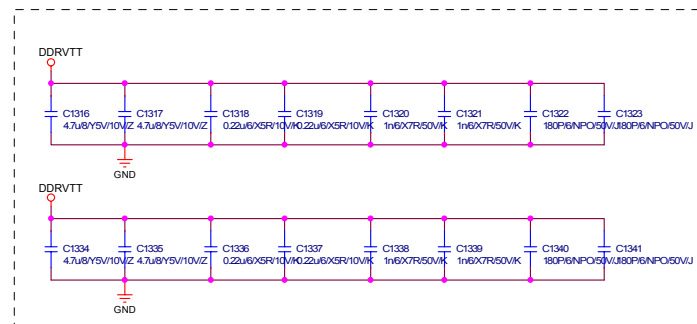
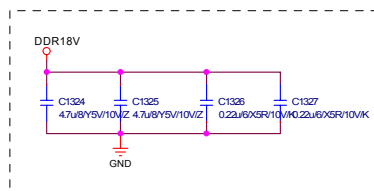
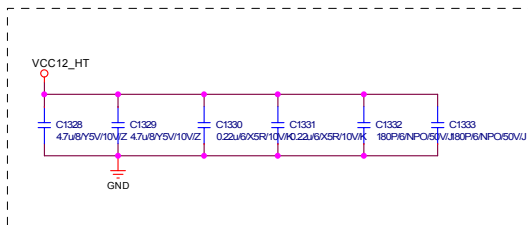
GIGABYTE

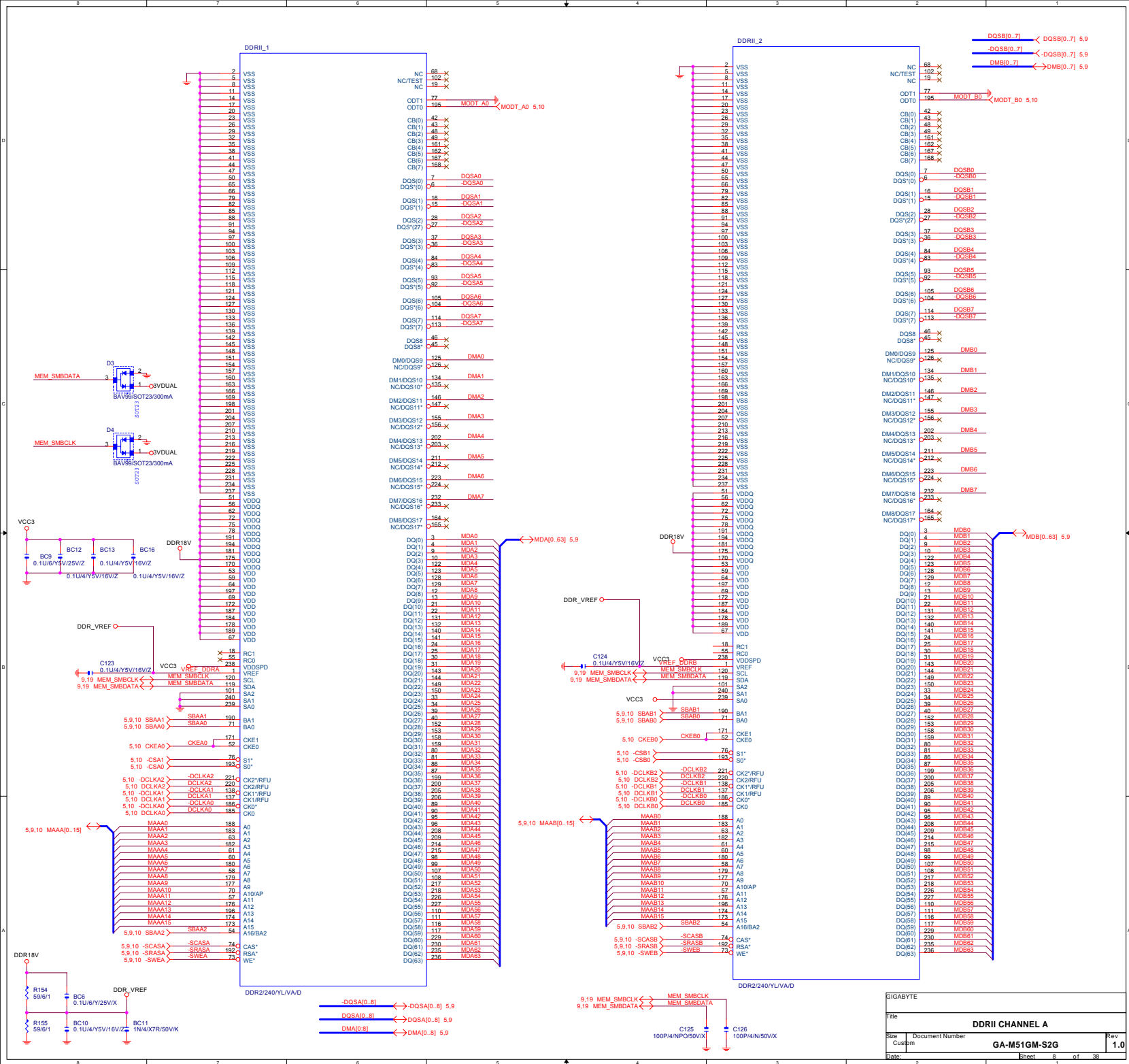
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Size	Document Number	Rev
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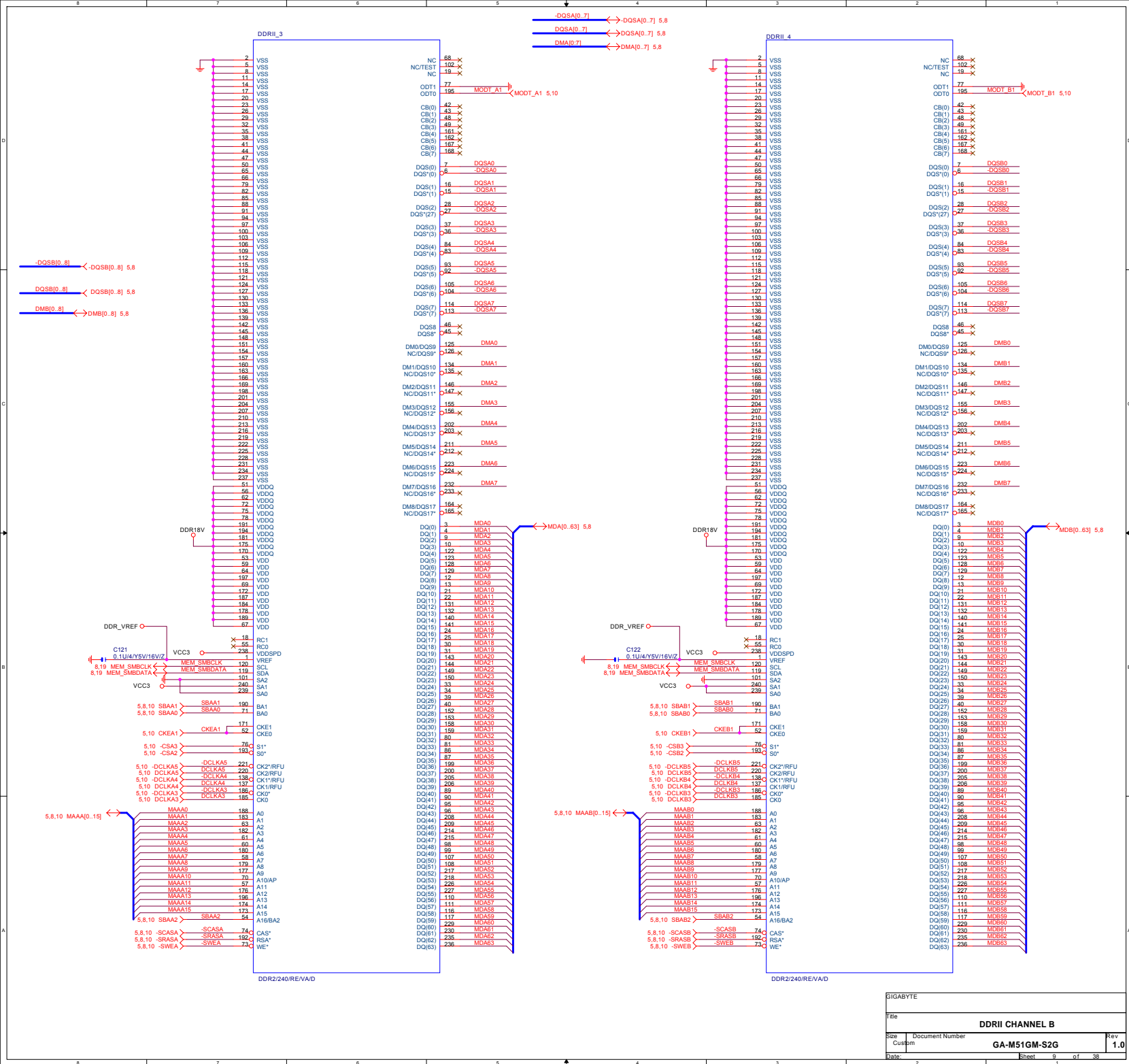


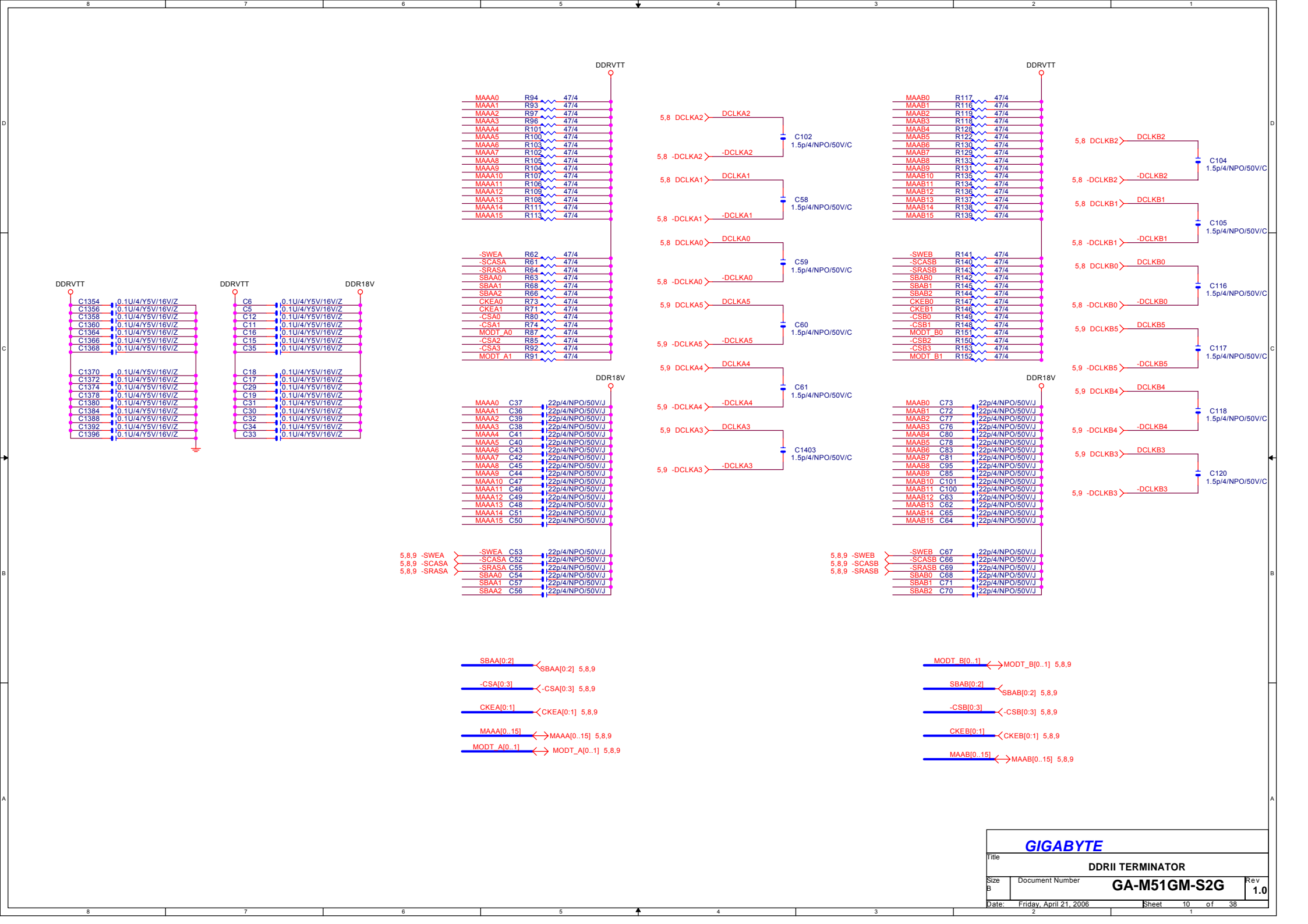


VLDT_RUN_B is connected to the VLDT_RUN power supply through the package or on the die. It is only connected on the board to decoupling near the CPU package.

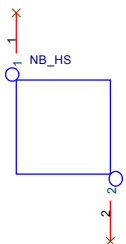






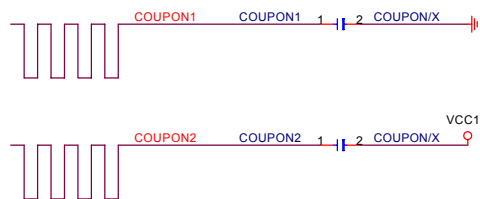
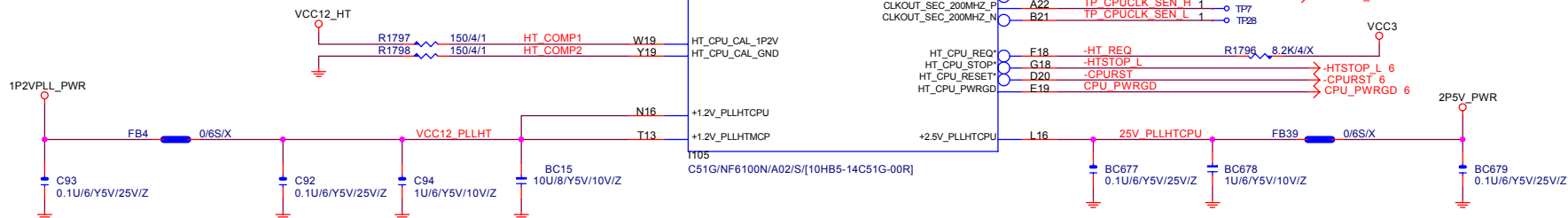


N.B HEATSINK



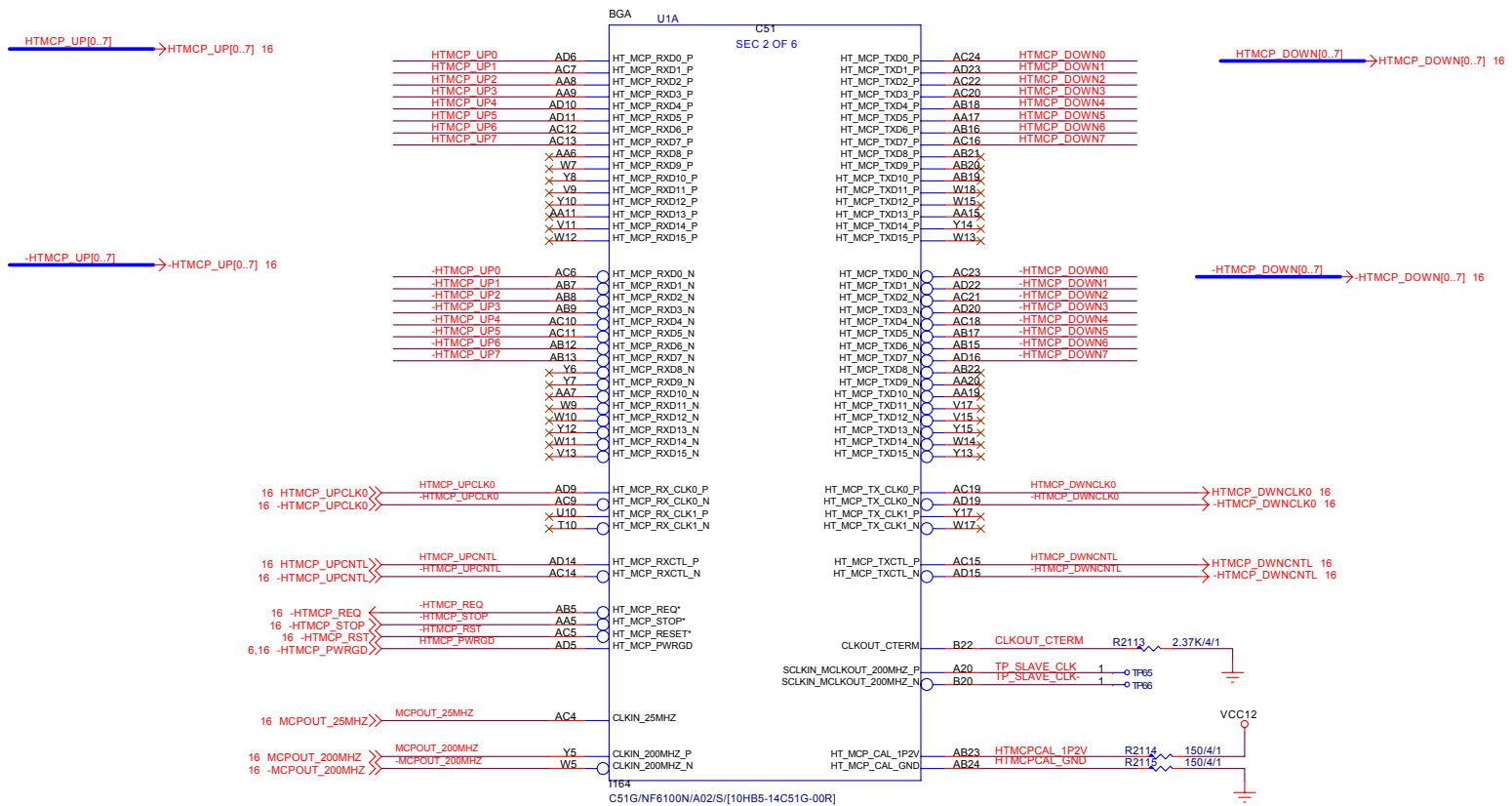
BGASINK_NB[12SP2-04E004-A1R_12SP2-04E004-A2R_12SP2-04E004-A3R_12SP2-04E004-A4R]

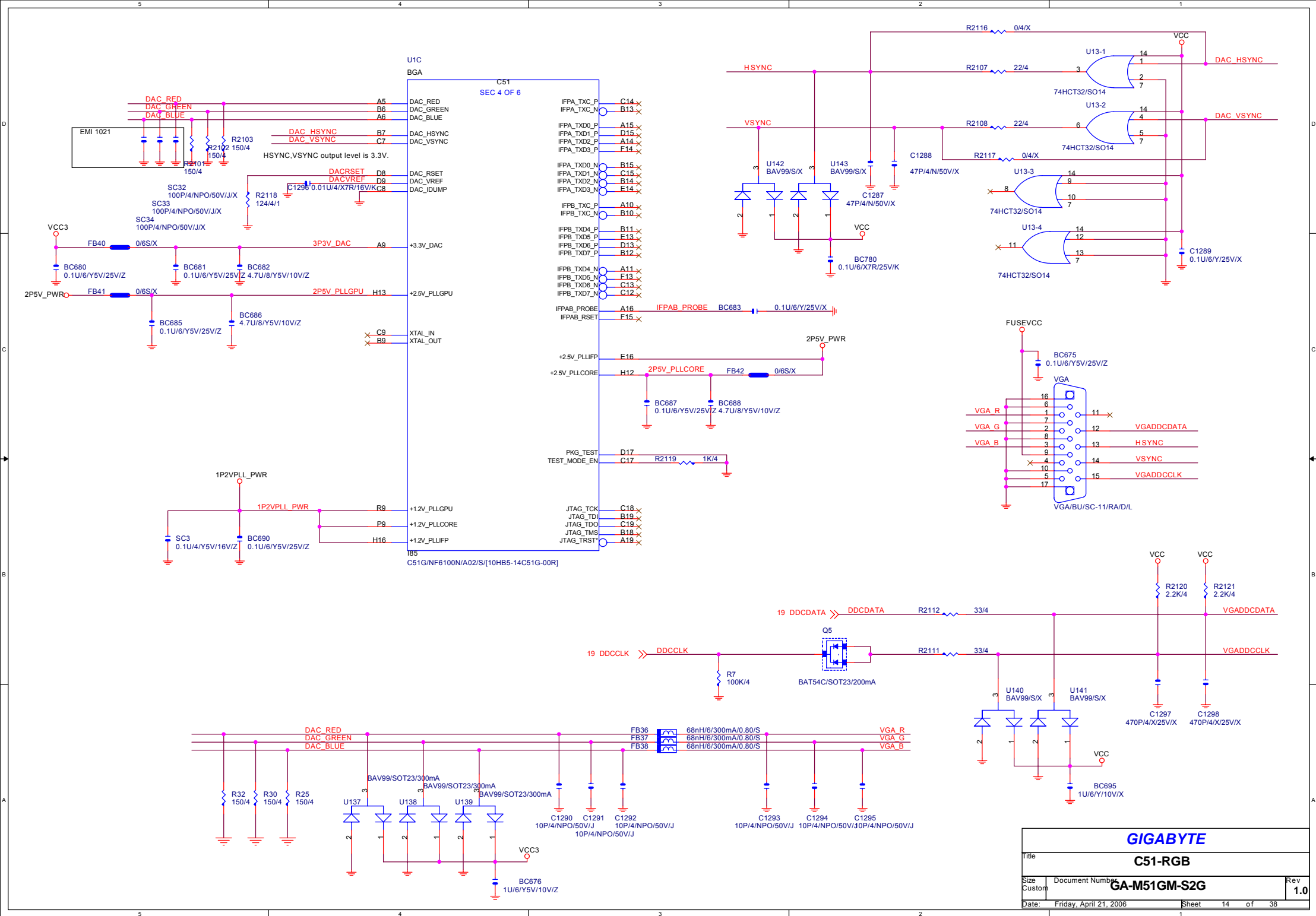
BGASINK_NB[12SP2-04F004-11_12SP2-04F004-12_12SP2-04F004-13]

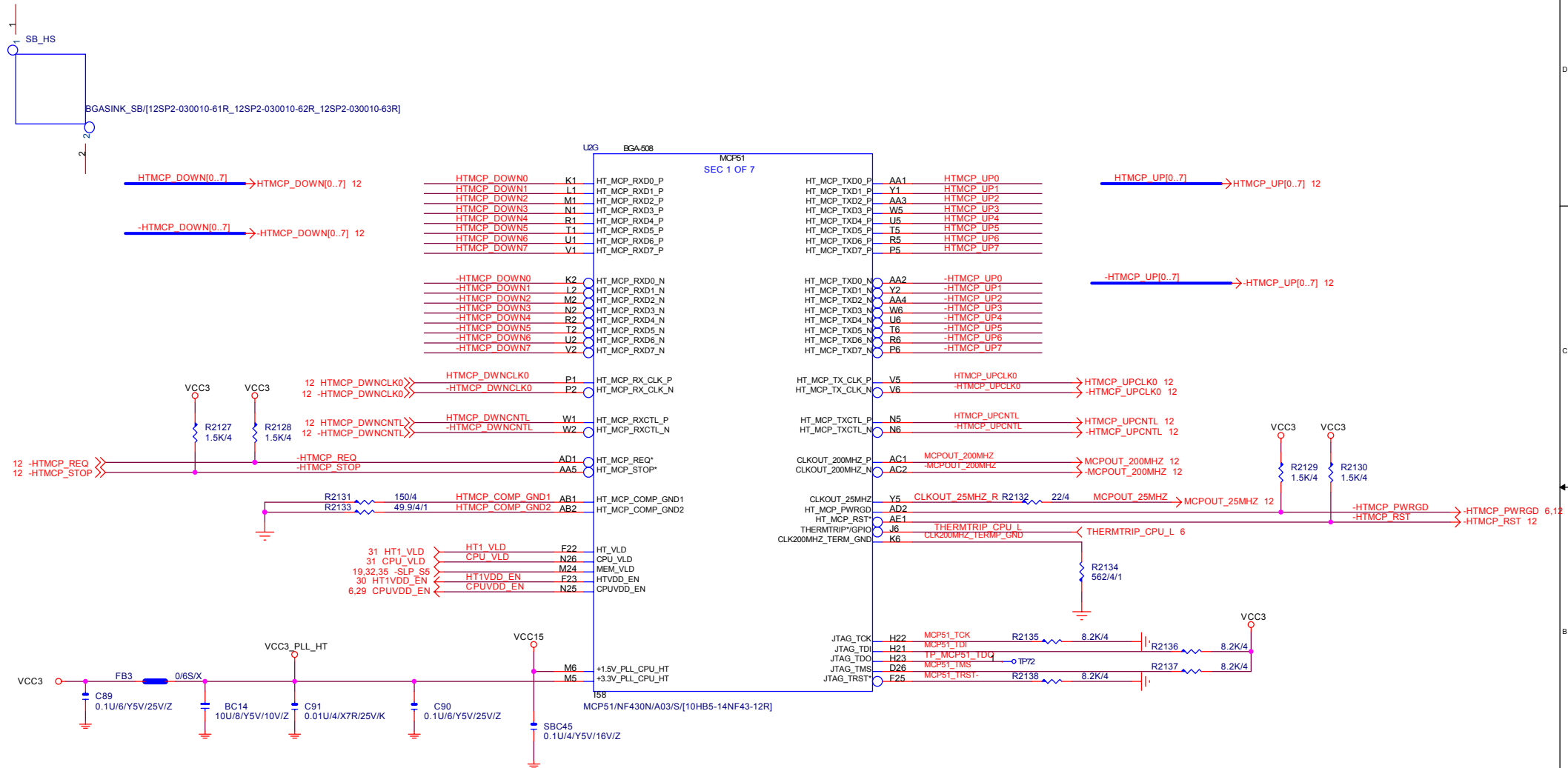


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C51-HOST			
GA-M51GM-S2G			
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24,38 AD[0..31] ←

AD0	AE19	PCL_AD0
AD1	AB21	PCL_AD1
AD2	AC19	PCL_AD2
AD3	AA20	PCL_AD3
AD4	AA19	PCL_AD4
AD5	AF20	PCL_AD5
AD6	AE19	PCL_AD6
AD7	AE20	PCL_AD7
AD8	AB20	PCL_AD8
AD9	AB19	PCL_AD9
AD10	AA18	PCL_AD10
AD11	AB18	PCL_AD11
AD12	AE18	PCL_AD12
AD13	AE18	PCL_AD13
AD14	AC17	PCL_AD14
AD15	AA17	PCL_AD15
AD16	AB15	PCL_AD16
AD17	AE15	PCL_AD17
AD18	AE15	PCL_AD18
AD19	AE14	PCL_AD19
AD20	AE14	PCL_AD20
AD21	AA14	PCL_AD21
AD22	AB14	PCL_AD22
AD23	AC13	PCL_AD23
AD24	AB13	PCL_AD24
AD25	AE13	PCL_AD25
AD26	AA12	PCL_AD26
AD27	AF13	PCL_AD27
AD28	AB12	PCL_AD28
AD29	AE12	PCL_AD29
AD30	AE12	PCL_AD30
AD31	AE11	PCL_AD31

24,38 -C_BE0 ← -C_BE0 AD19 PCL_CBE0*
24,38 -C_BE1 ← -C_BE1 AB17 PCL_CBE1*
24,38 -C_BE2 ← -C_BE2 AA15 PCL_CBE2*
24,38 -C_BE3 ← -C_BE3 AA13 PCL_CBE3*

24,38 -FRAME ← -FRAME AC15 PCL_FRAME*
24,38 -IRDY ← -IRDY AD15 PCL_IRDY*
24,38 -TRDY ← -TRDY AB16 PCL_TRDY*
24,38 -STOP ← -STOP AE16 PCL_STOP*
24,38 -DEVSEL ← -DEVSEL AA16 PCL_DEVSEL*
24,38 PAR ← PAR AE17 PCL_PAR
24,38 -PERR ← -PERR AE16 PCL_PERR*/GPIO
24,38 -SERR ← -SERR AE17 PCL_SERR*
24,38 -PCIPME ← -PCIPME AD11 PCL_PME*/GPIO
VCC3 R70 8.2K/4 -PCI_CLKRUN ← -PCI_CLKRUN AE25 PCL_CLKRUN*/GPIO

24 -PPCIRST ← -PPCIRST R79 33/4 AE25 PCL_RESET0*
38 -1394RST ← -1394RST R81 33/4 AD24 PCL_RESET1*
28 -IDERST ← -IDERST R82 33/4 AE26 PCL_RESET2*
36 -LPCRST ← -LPCRST R83 33/4 L26 PCL_RESET3*
33 -BIOSRST ← -BIOSRST R114 33/4 L26 PCL_RESET3*

MCP51/NF430N/A03/S/[10HB5-14NF43-12R]

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PCL_REQ0* AA22 -REQ0 → REQ0 24
PCL_REQ1* AE22 -REQ1 → REQ1 24
PCL_REQ2* AE21 -REQ2 → REQ2 24,38
PCL_REQ3*/GPIO AE22 -REQ3 → REQ3 24
PCL_REQ4*/GPIO AE23 -REQ4 → REQ4 24

PCL_GNT0* AE21 -GNT0 → GNT0 24
PCL_GNT1* AC21 -GNT1 → GNT1 24
PCL_GNT2* AA21 -GNT2 → GNT2 24,38
PCL_GNT3*/GPIO AB24 -GNT3 → GNT3 24,38
PCL_GNT4*/GPIO AB22 -GNT4 → GNT4 24

PCL_INTW* AE11 -INTA → INTA 24
PCL_INTX* AB11 -INTB → INTB 24
PCL_INTY* AC11 -INTC → INTC 24,38
PCL_INTZ* AA11 -INTD → INTD 24

PCL_CLK0 AE24 PCLK0 R67 22/4 PCICLK1 24
PCL_CLK1 AF24 PCLK1 R69 22/4 PCICLK2 24
PCL_CLK2 AD23 PCLK2 R72 22/4 1394CLK 38
PCL_CLK3 AF23 PCLK3 R227 22/4
PCL_CLK4 AB23 PCLK4 R227 22/4

PCL_CLKIN AC23 PCICLK_FB

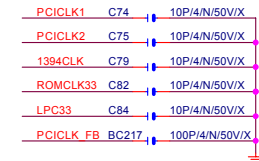
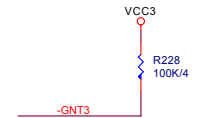
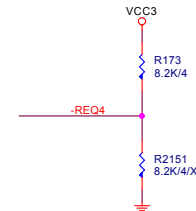
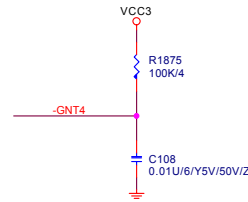
LPC_AD0 K24 LAD0 → LAD[0..3] 33,38
LPC_AD1 H26 LAD1 → LAD[0..3] 33,38
LPC_AD2 H25 LAD2 → LAD[0..3] 33,38
LPC_AD3 K22 LAD3 → LAD[0..3] 33,38

LPC_FRAME* G25 -LFRAME → LFRAME 33,38
LPC_DRQ0* K21 -LDRQ0 → LDRQ0 36 R76 8.2K/4 VCC3
LPC_DRQ1*/LPC_CS* K23 -LDRQ1 → LDRQ1 36
LPC_SERIRQ L22 SERIRQ → SERIRQ 36

LPC_PWRDWN*/GPIO H24 -TP LPC_PWRDWN 1 TP15

LPC_CLK0 F26 R84 22/4 LPC33 → LPC33 36

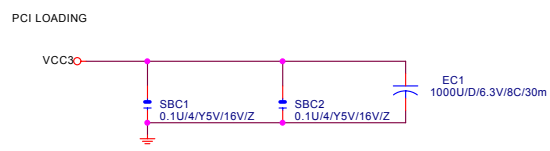
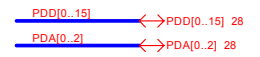
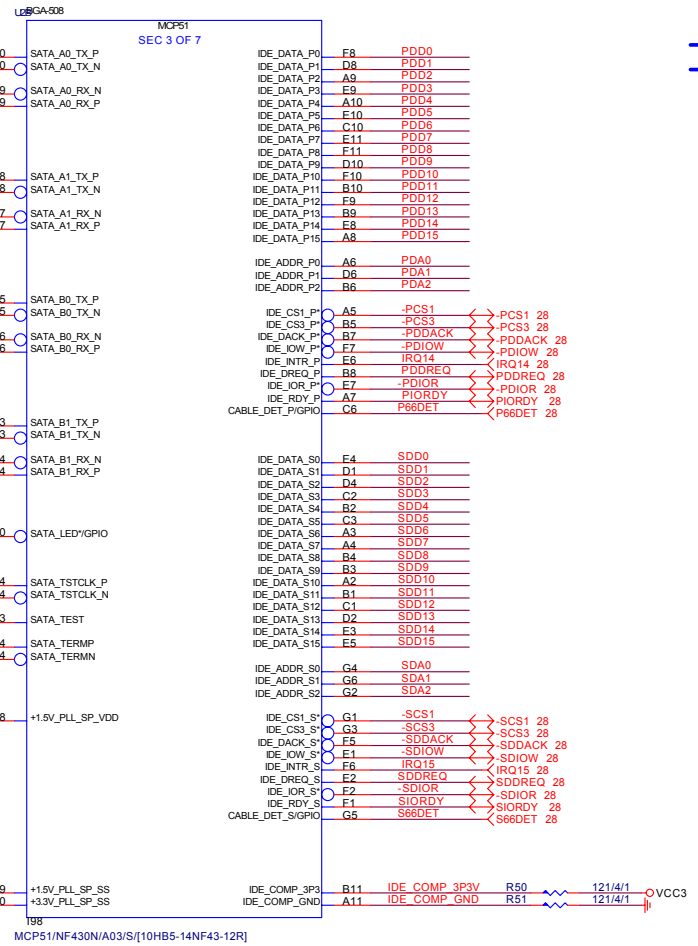
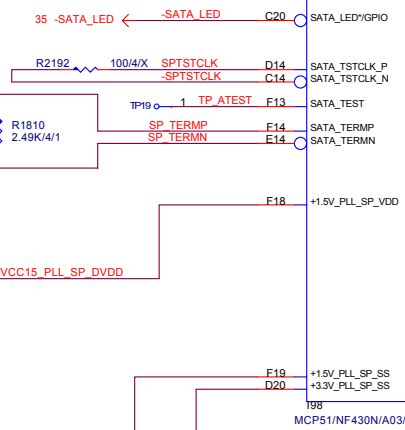
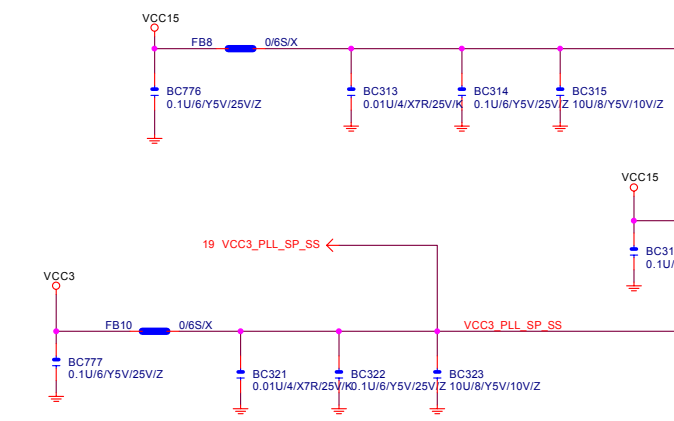
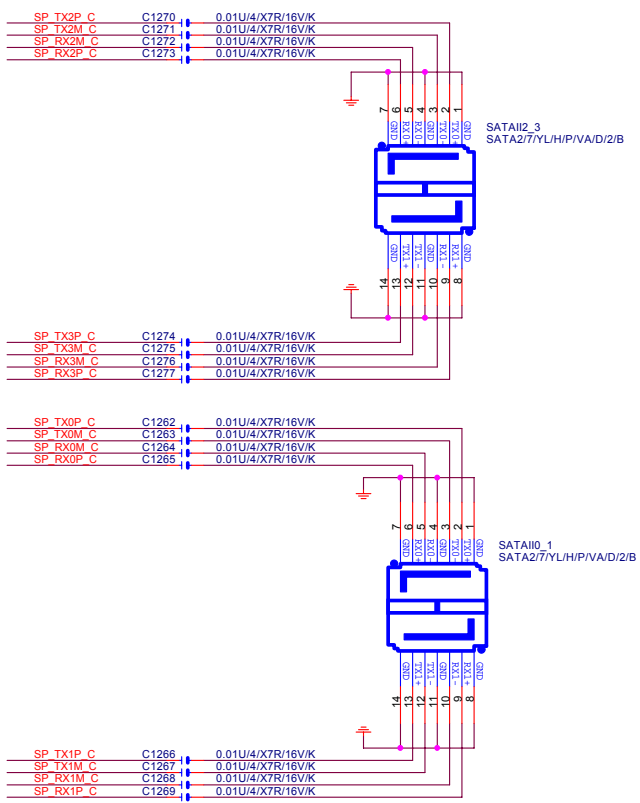
LPC_CLK1 G26 R86 22/4 ROMCLK33 → ROMCLK33 33

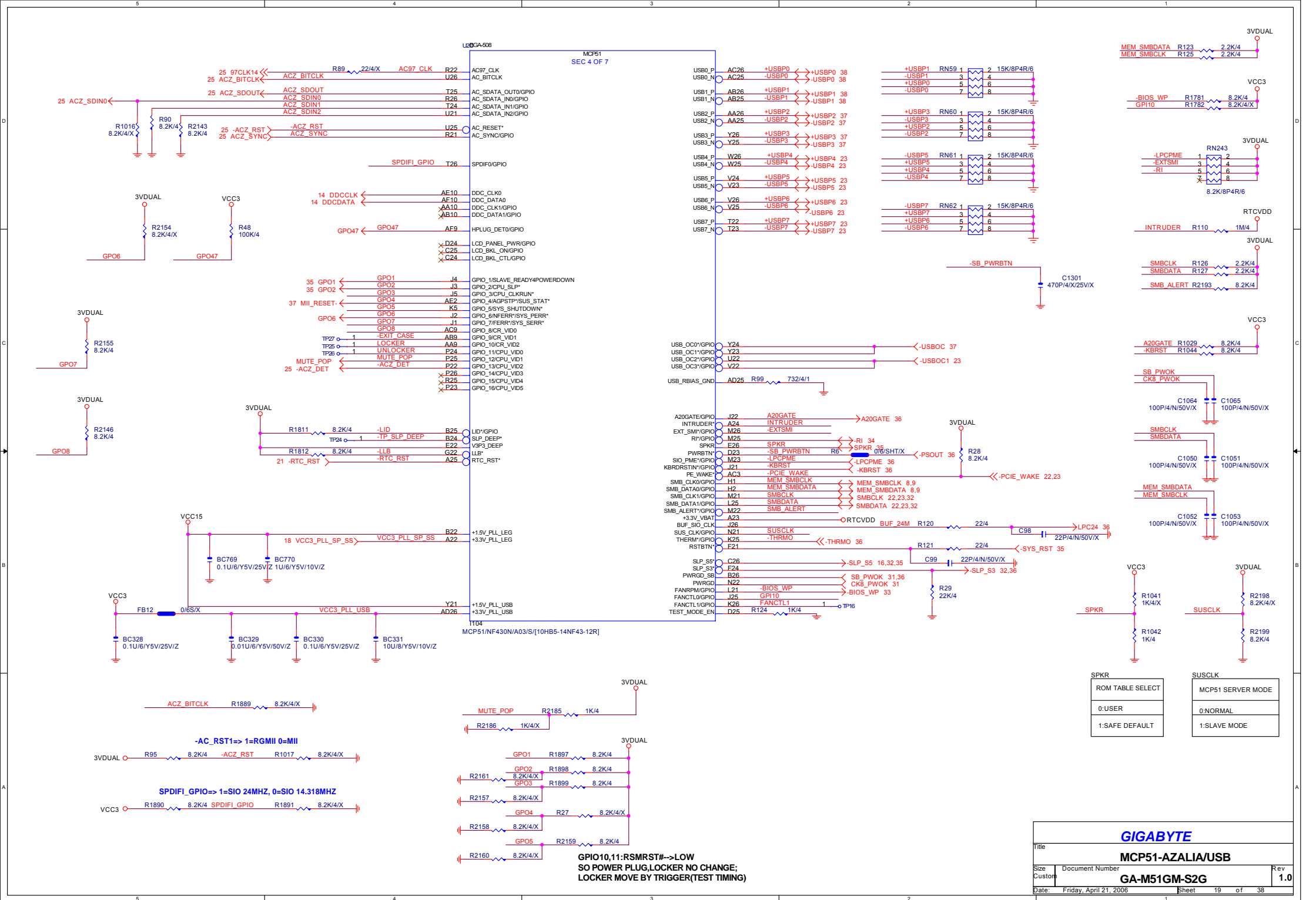


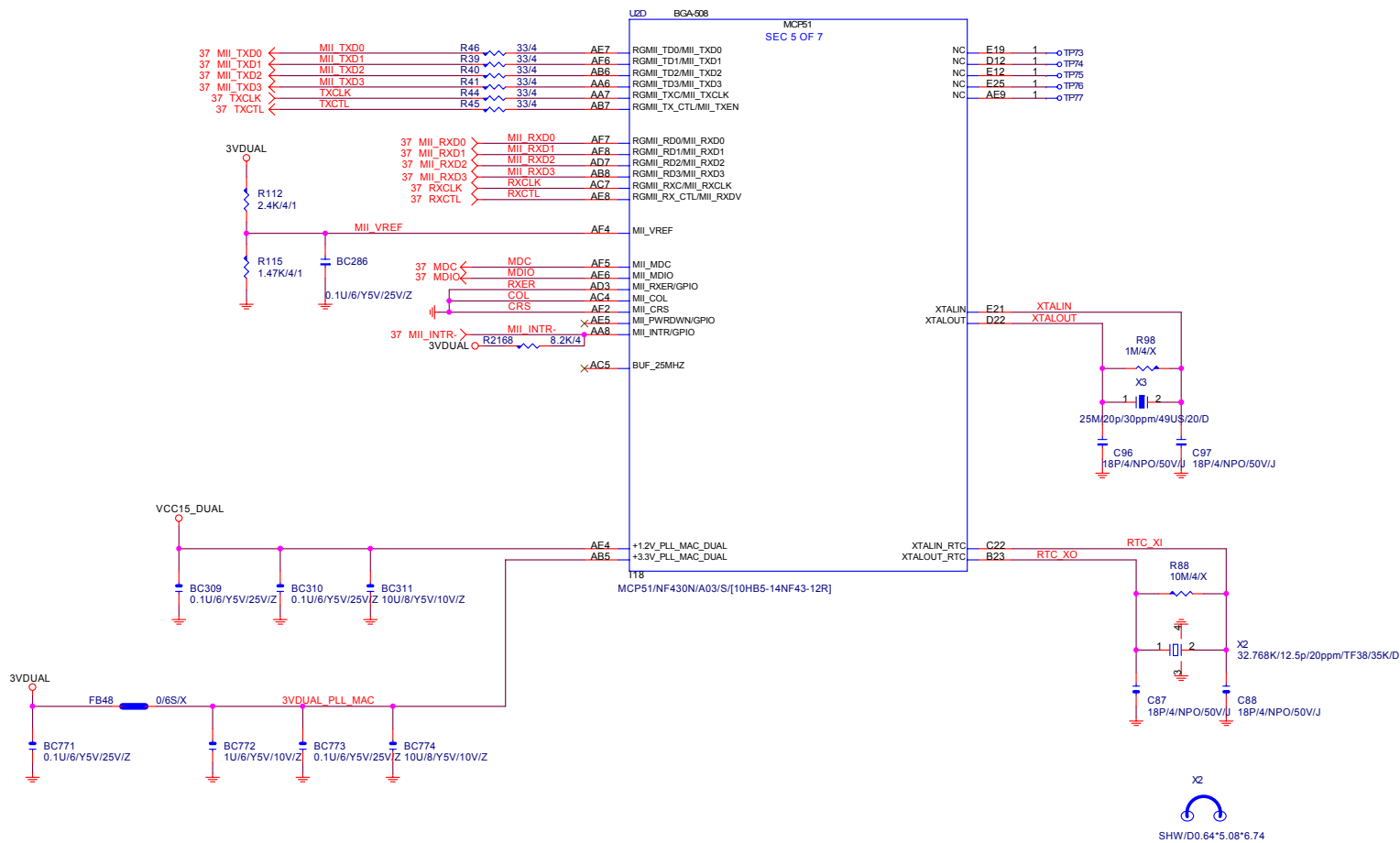
SERIRQ R75 8.2K/4 VCC3
-LDRQ0 R77 8.2K/4 VCC3
-PCIPME R78 8.2K/4 3VDUAL

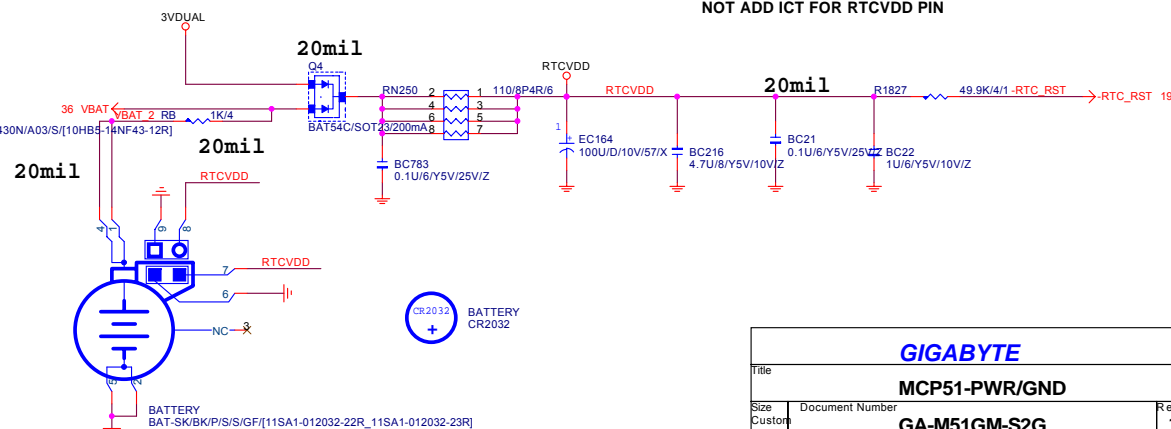
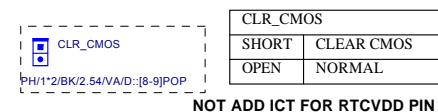
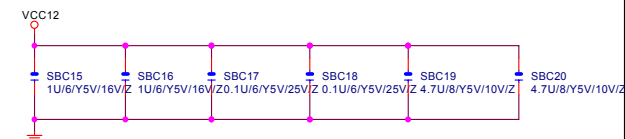
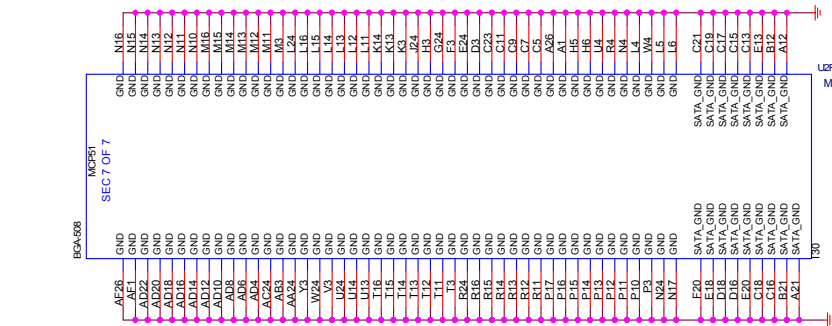
GIGABYTE

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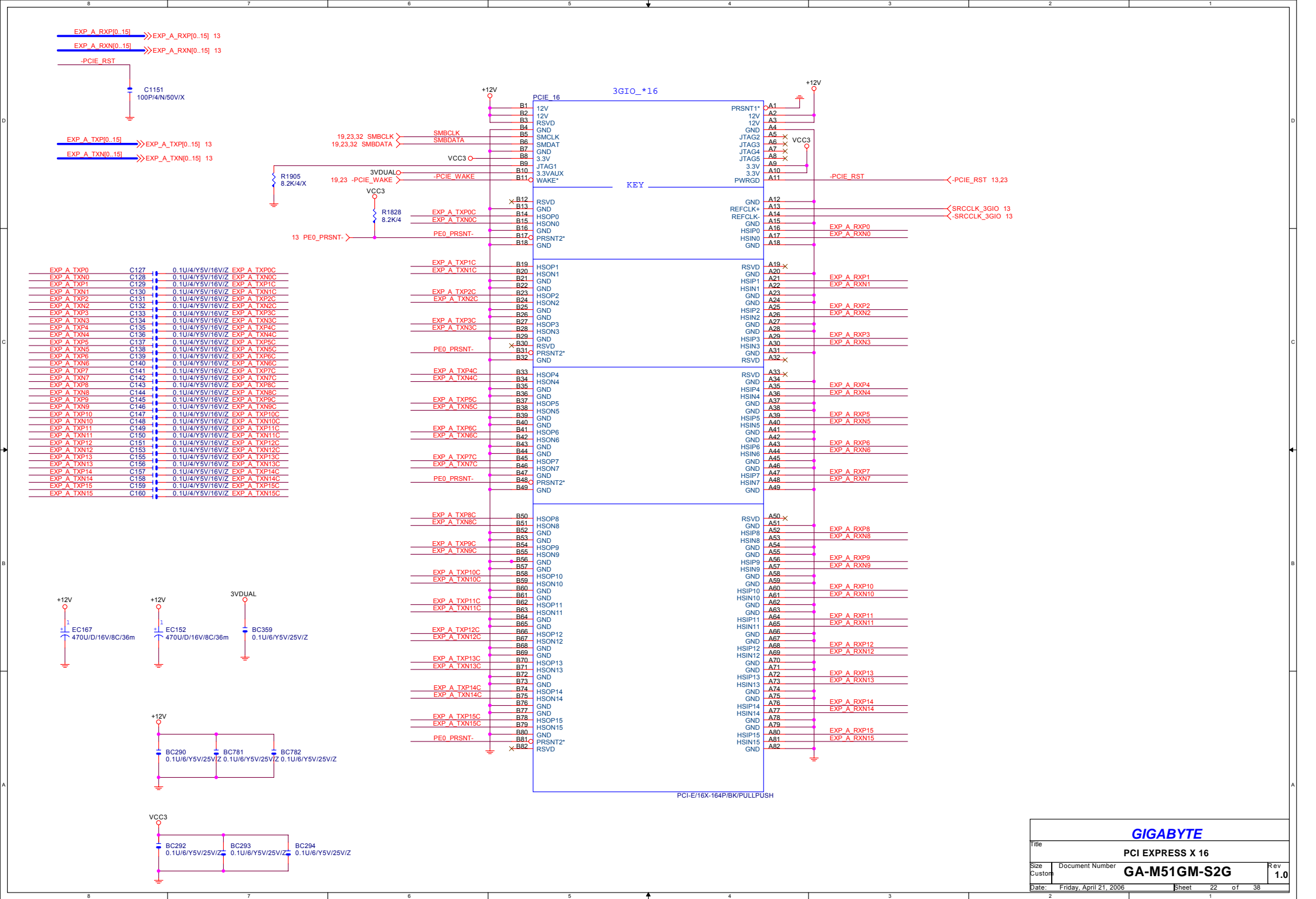




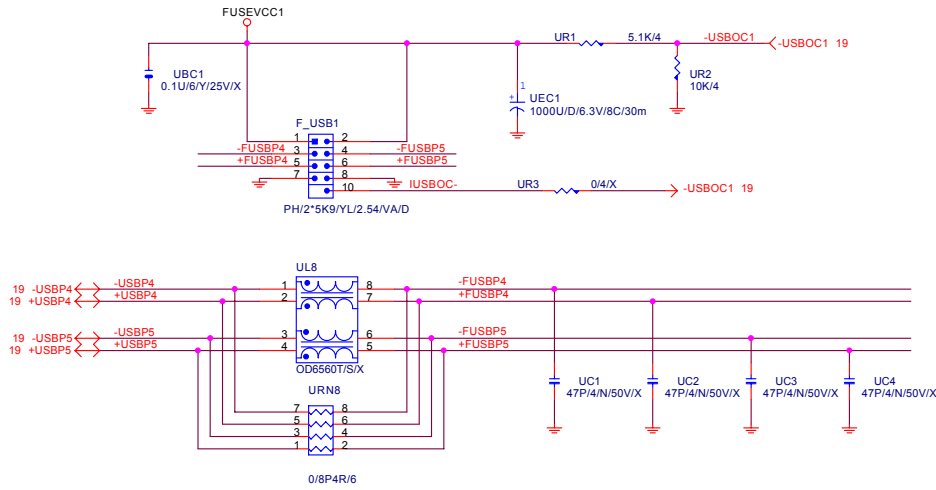




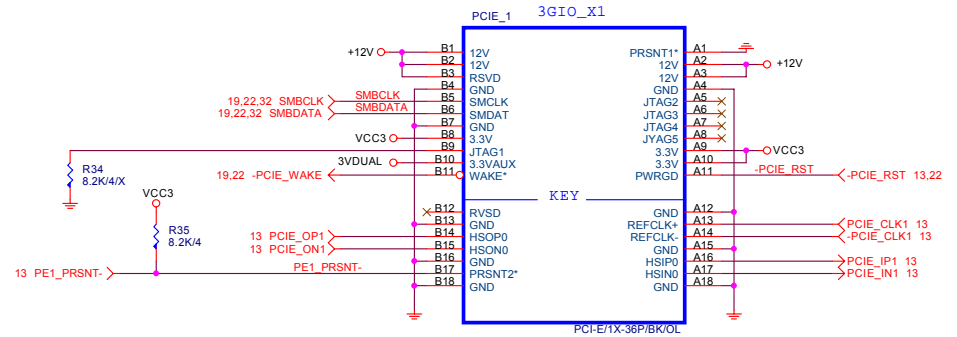
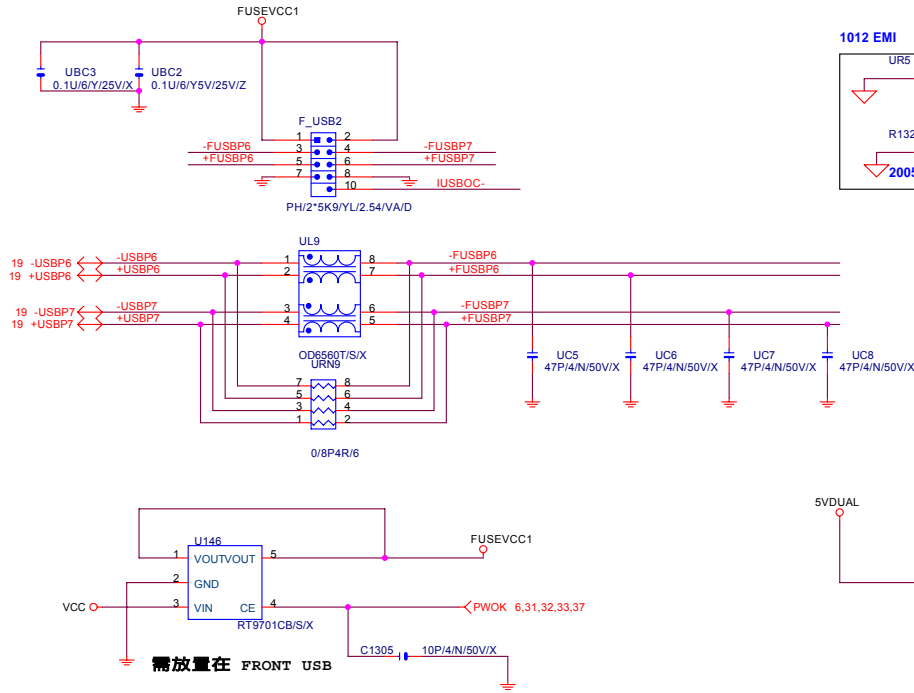
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MCP51-PWR/GND			
Size	Document Number		Rev
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FRONT SIDE USB1

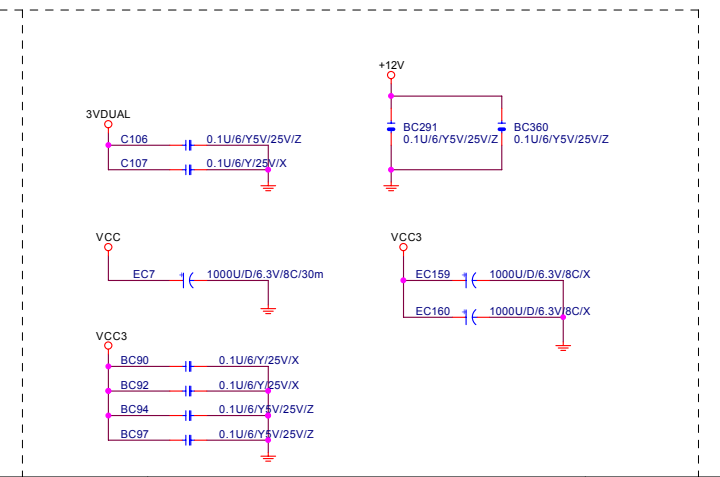
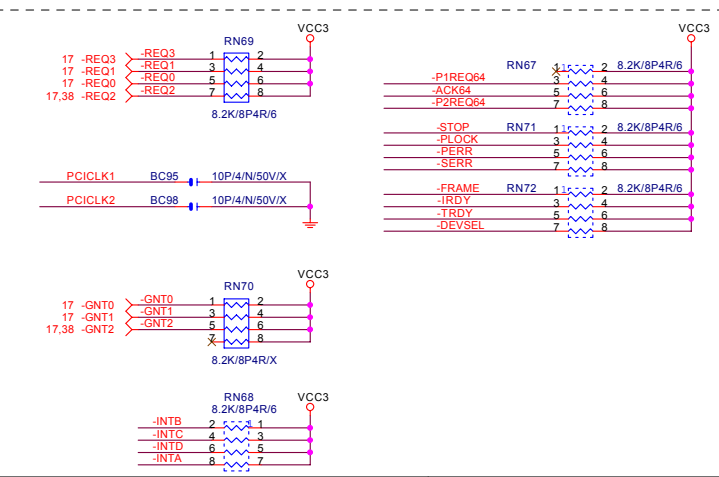
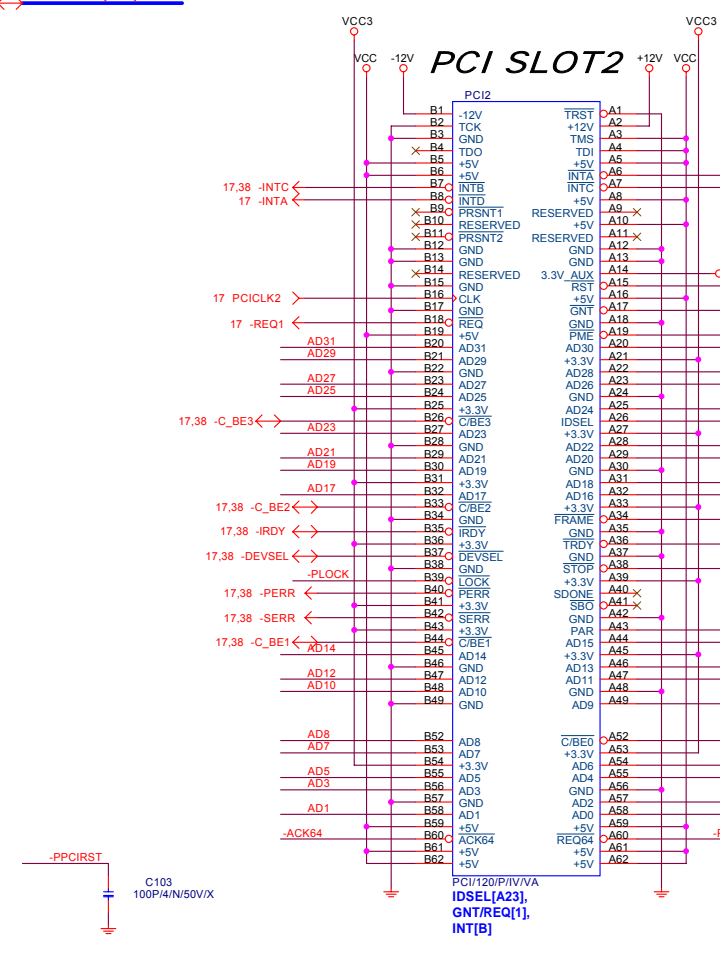
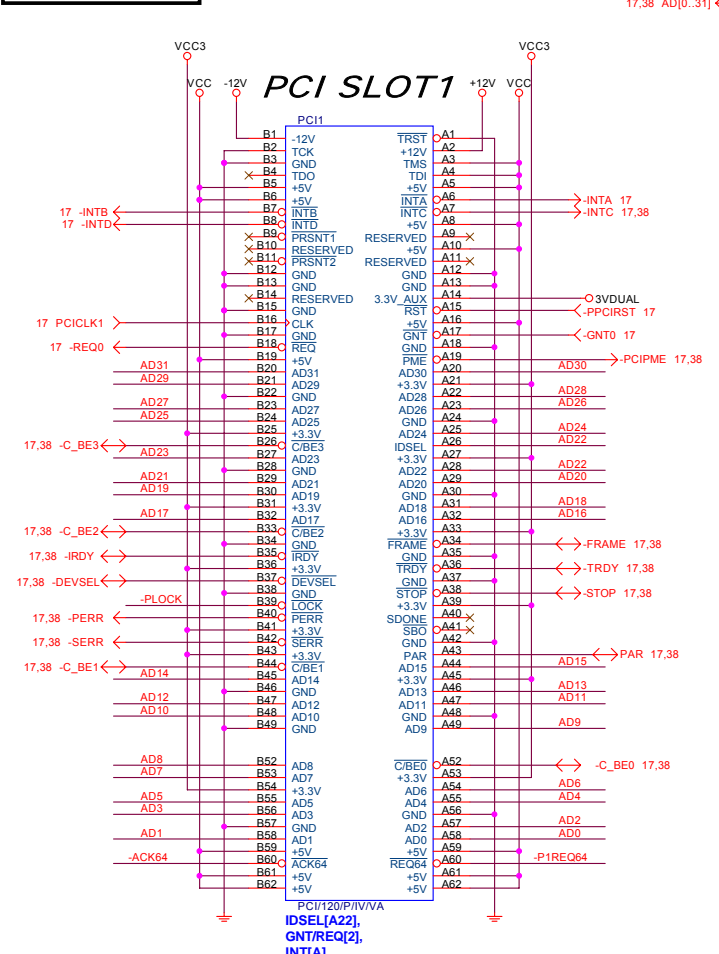


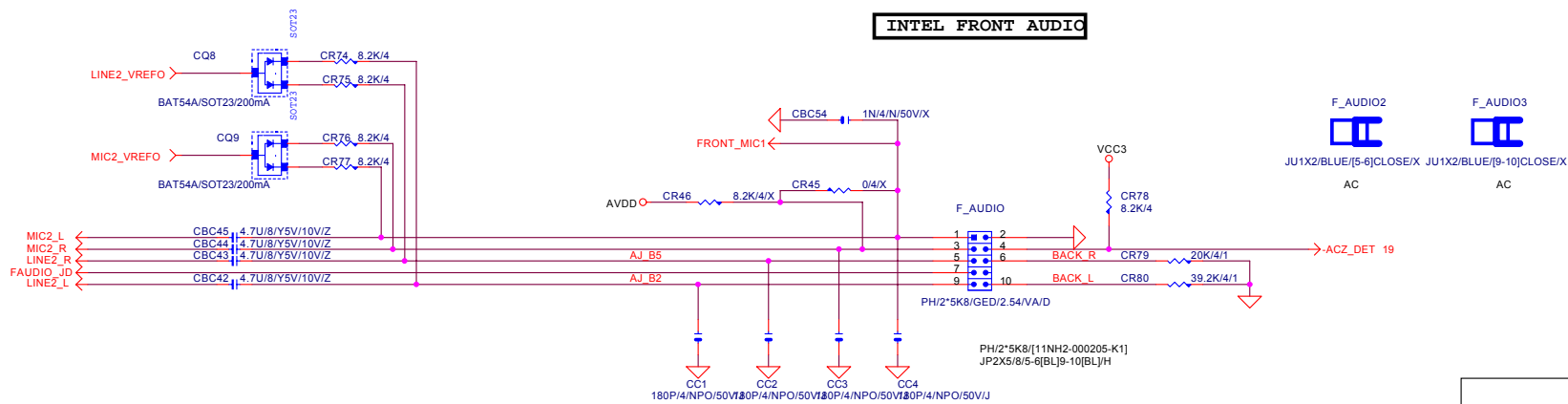
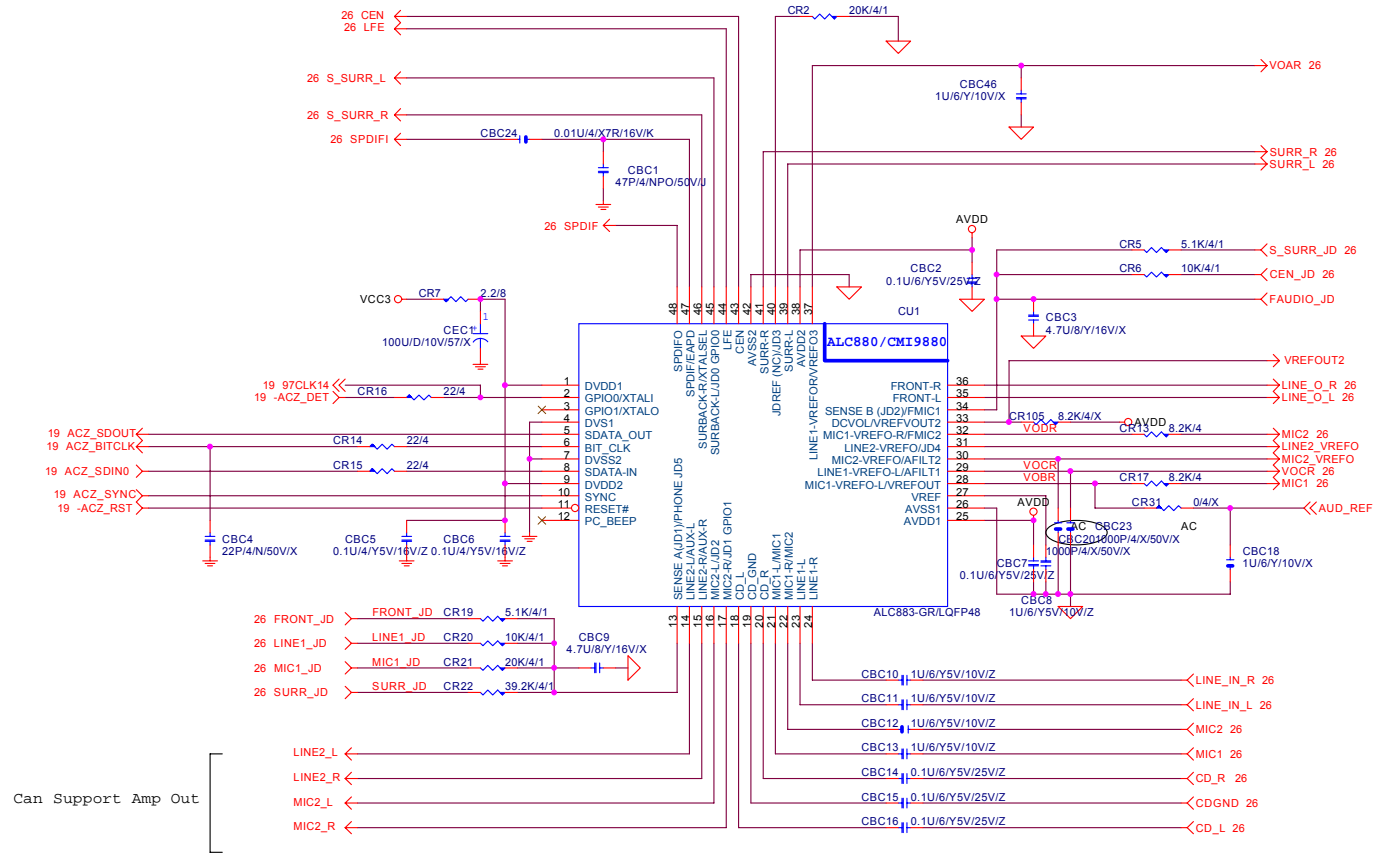
FRONT SIDE USB2



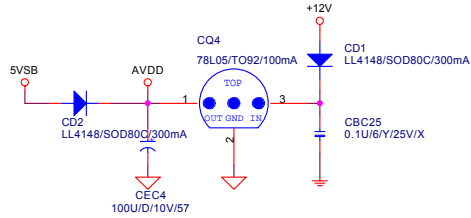
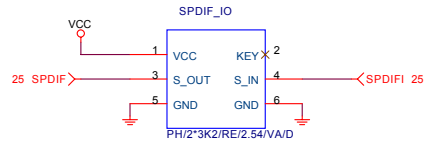
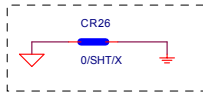
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PCI_EX X1 USB PORT			
Size	Document Number	Rev	
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PCI SLOT 1,2,3

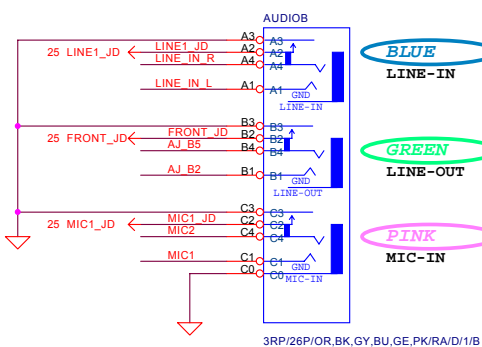
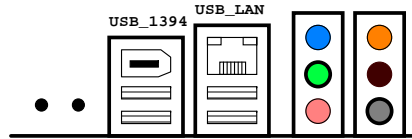
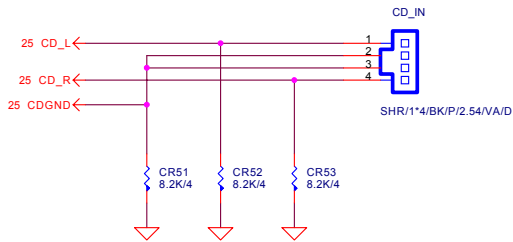




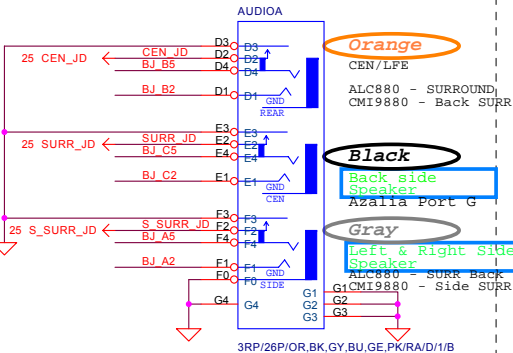
GIGABYTE			
Title			
ALC883			
Size	Document Number	GA-M51GM-S2G	
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CD IN

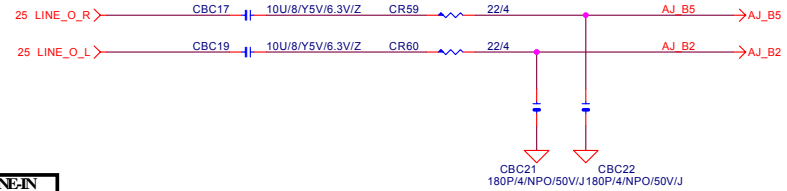


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3RJ+15F/[11NR6-403004-11]

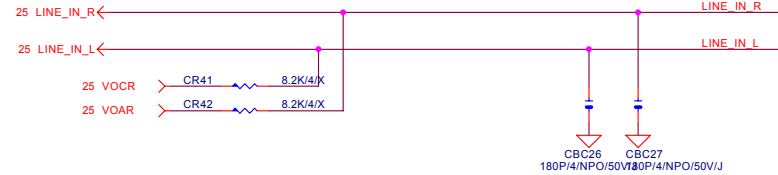


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3RJ+15F/[11NR6-403004-31]

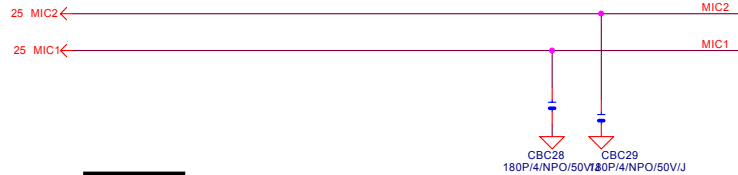
LINE OUT FRONT OUT



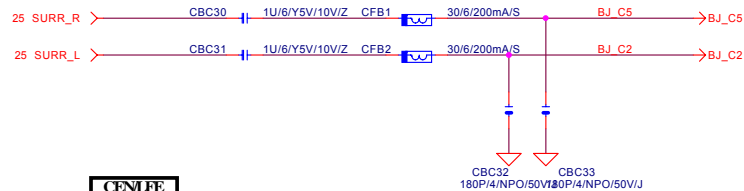
LINE IN



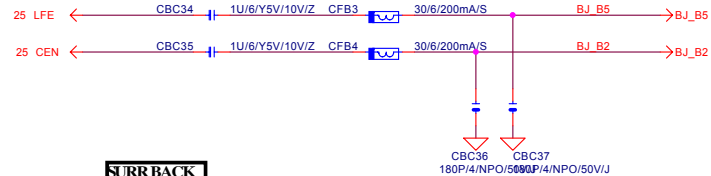
MIC



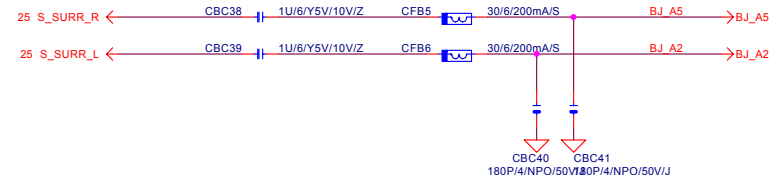
SURROUND



CEN/LFE



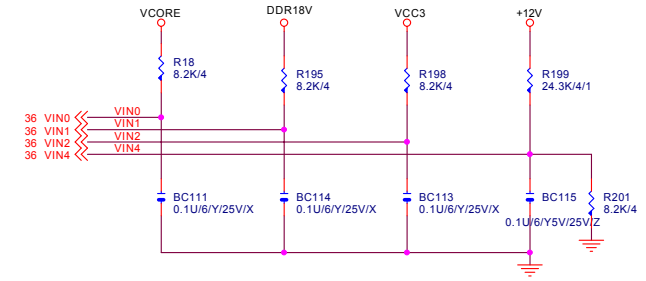
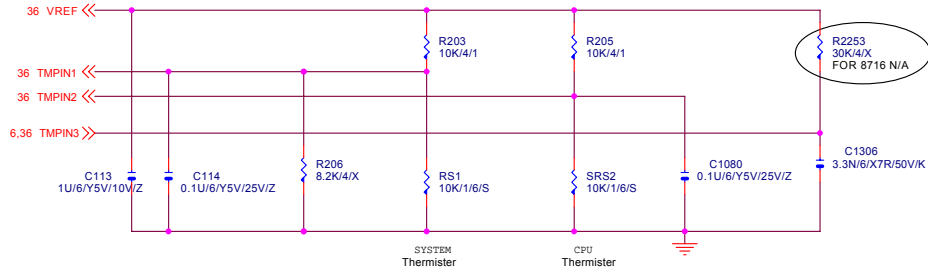
SURR BACK



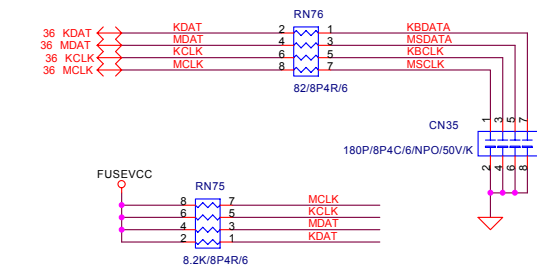
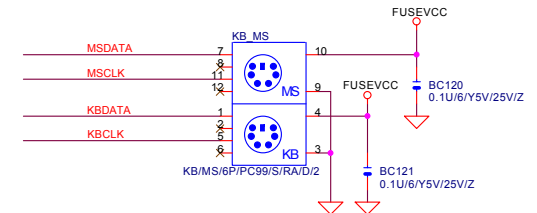
GIGABYTE

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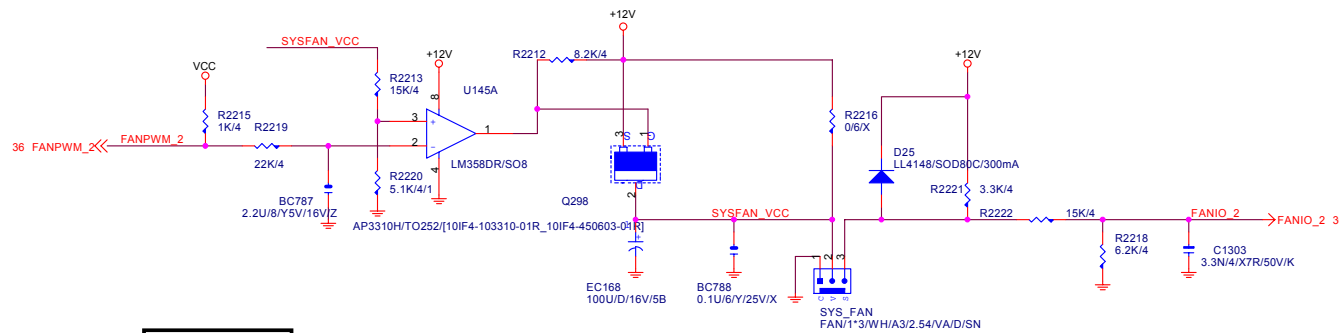
Hardware Monitor circuits



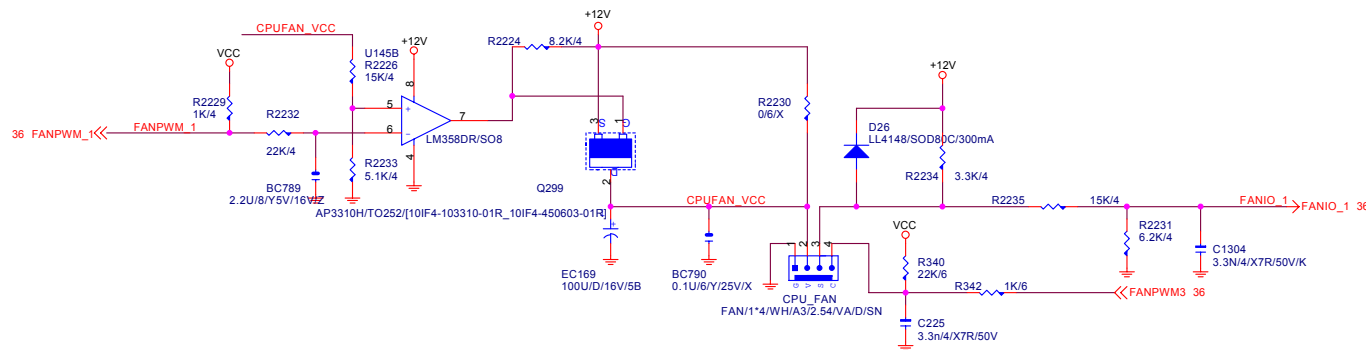
KB & MS



SYSTEM FAN

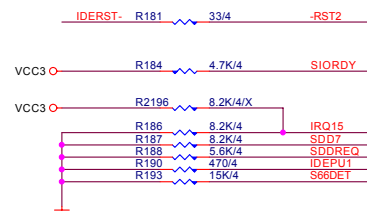
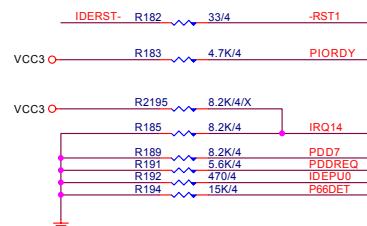
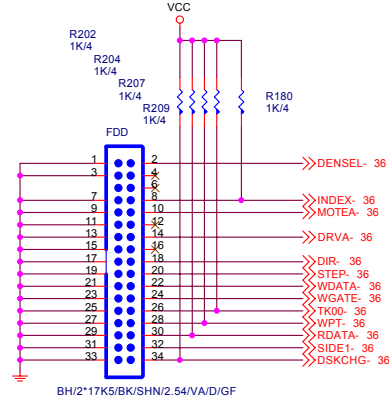
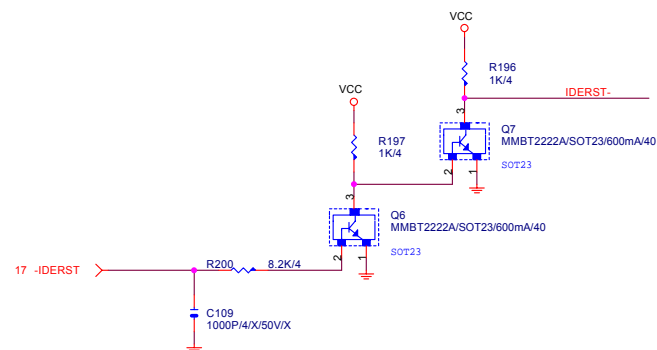


CPU FAN

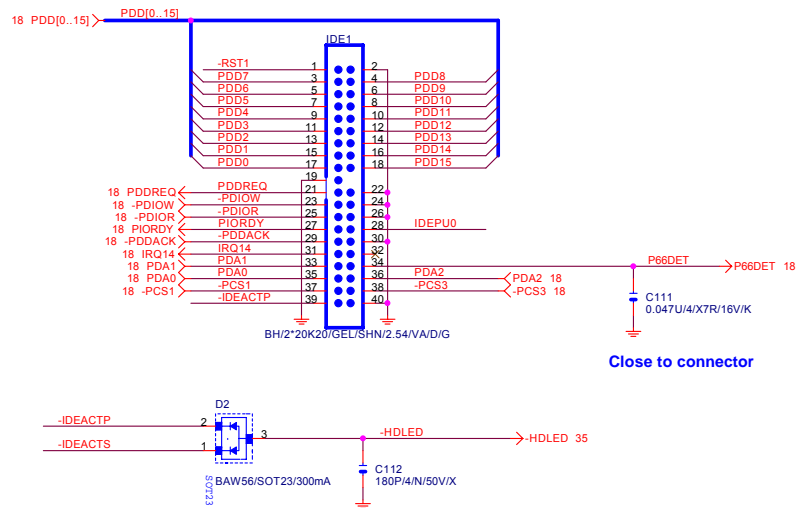


GIGABYTE

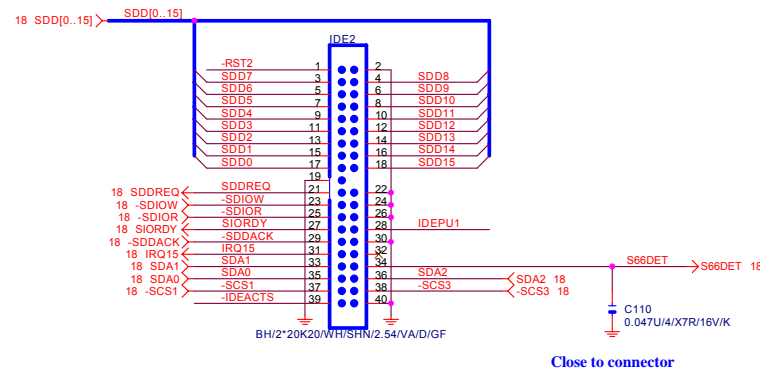
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FAN/HWMO KB/MS			
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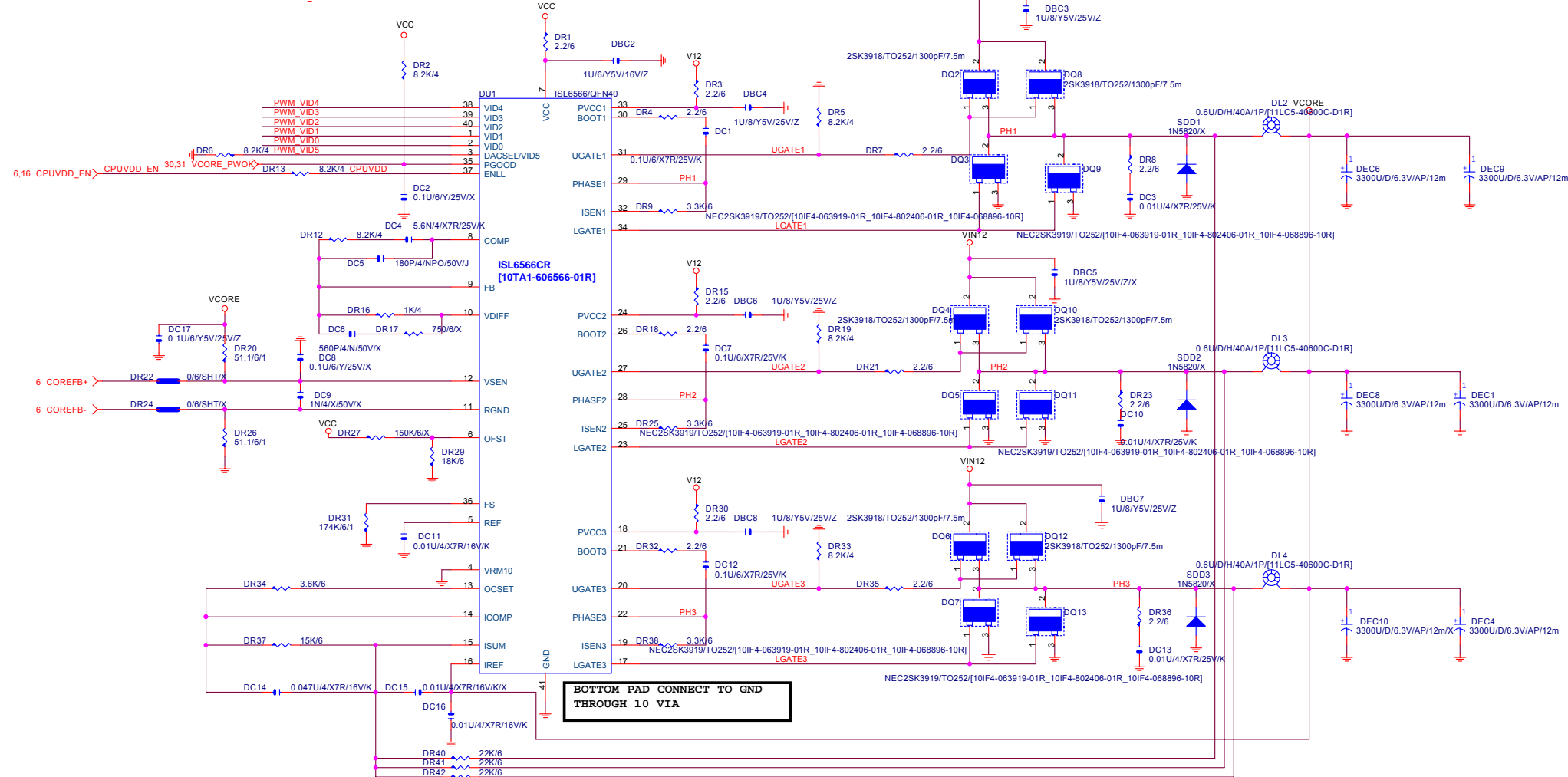
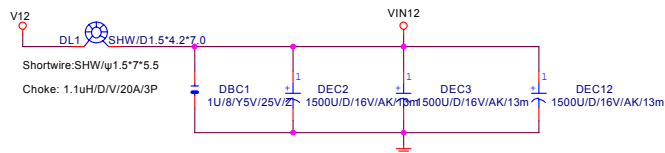


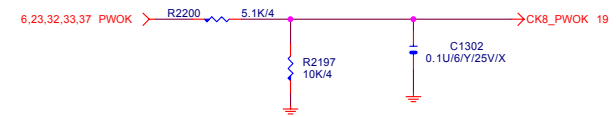
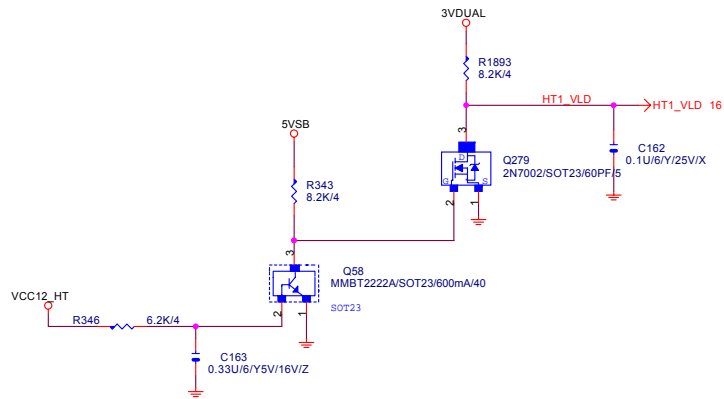
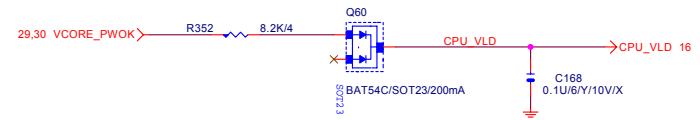
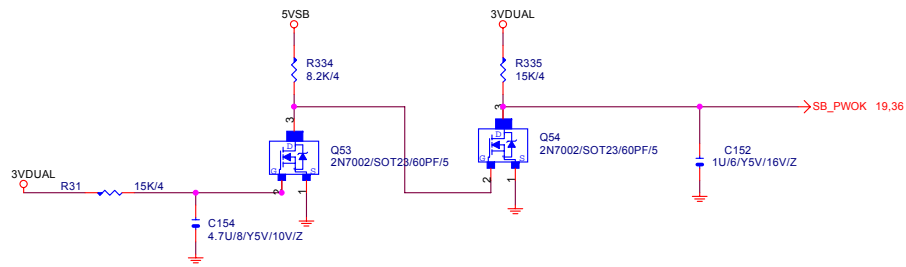
PRIMARY IDE CONNECTOR



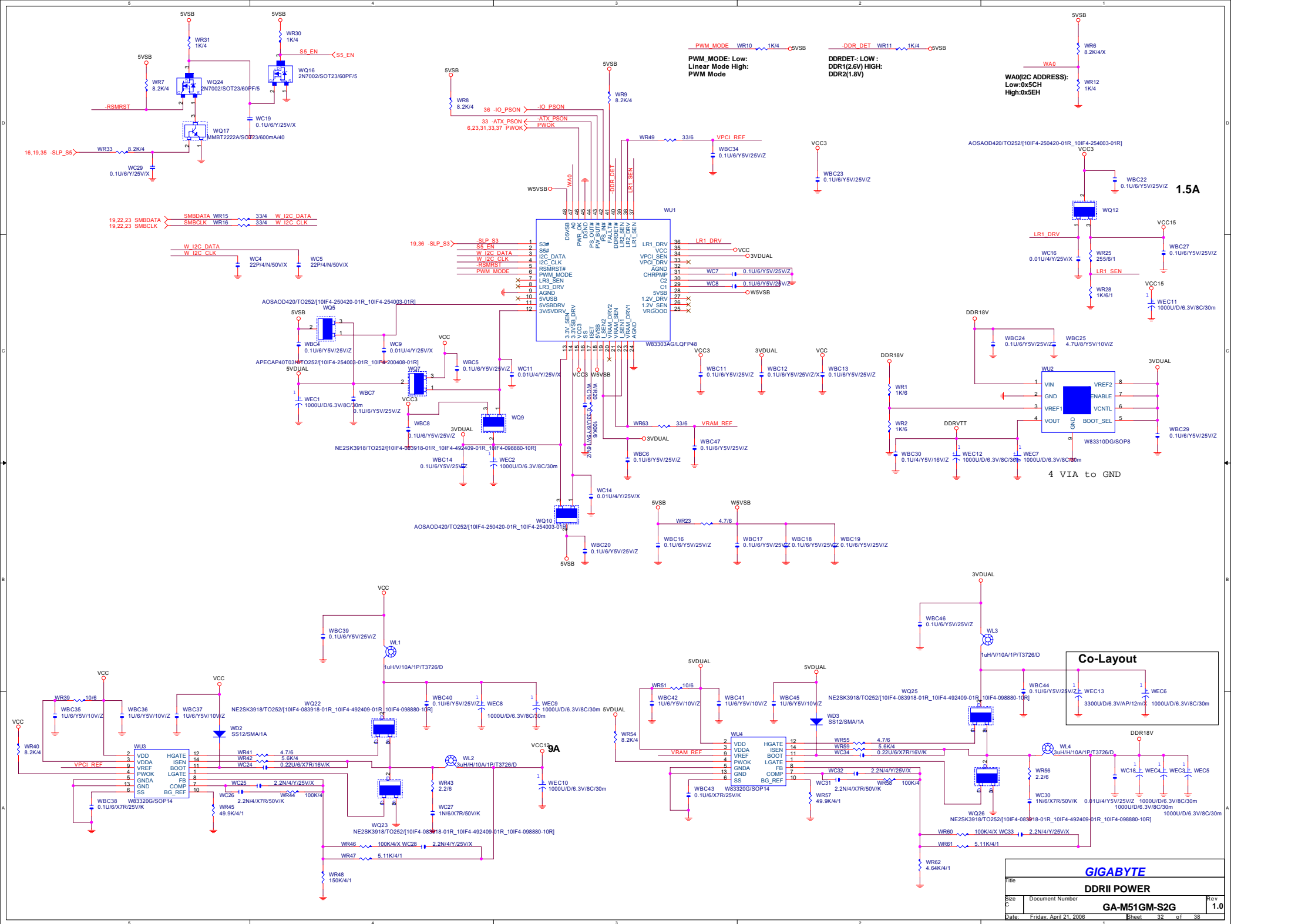
SECONDARY IDE CONNECTOR



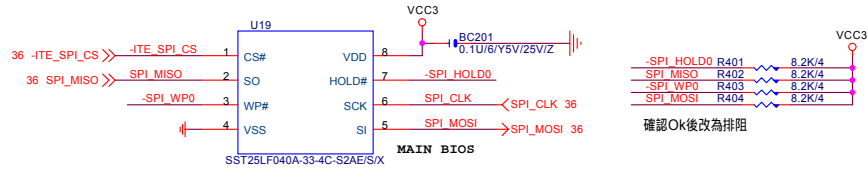
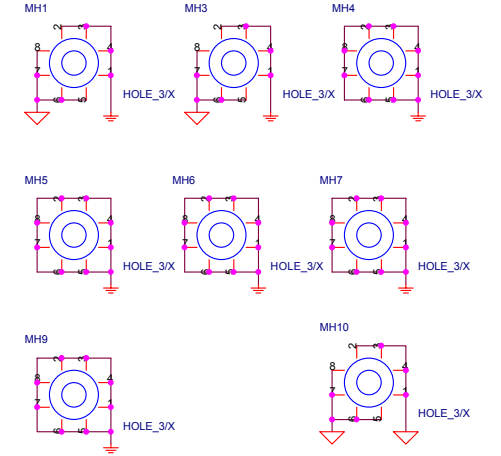
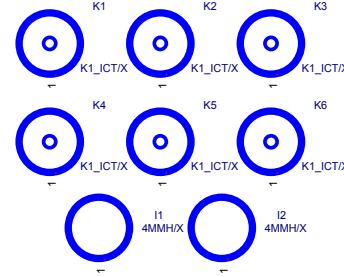
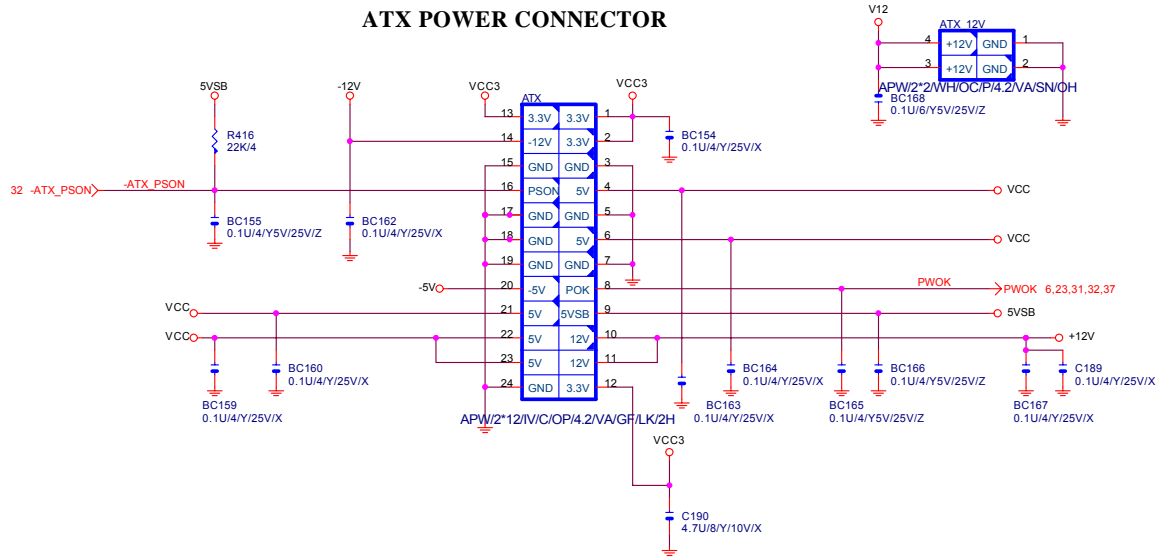




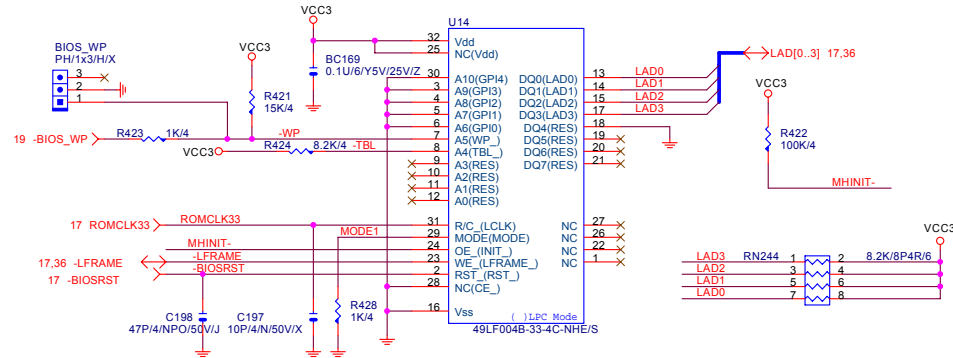
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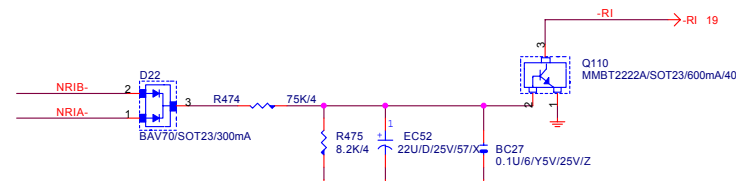
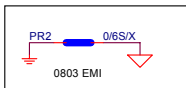
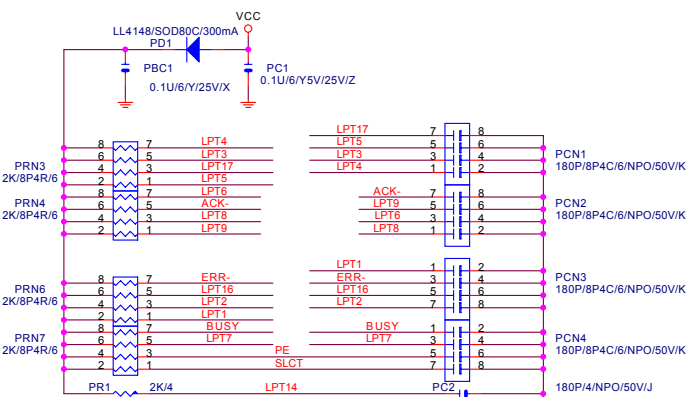
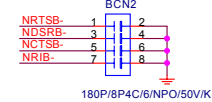
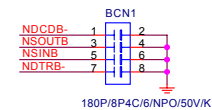
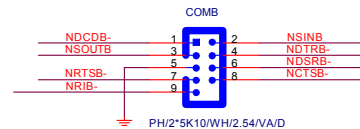
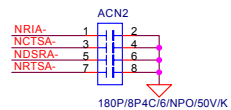
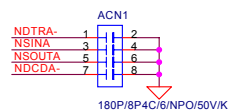
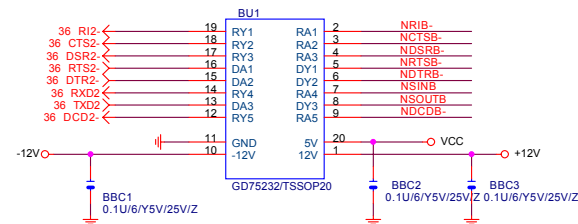
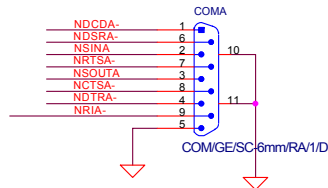
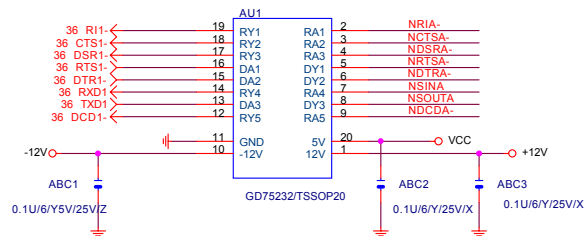


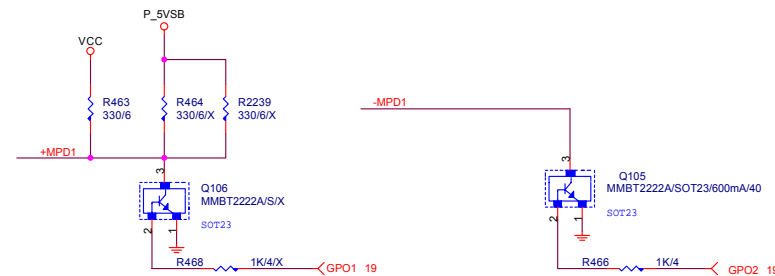
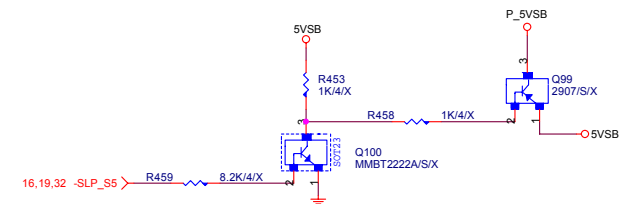
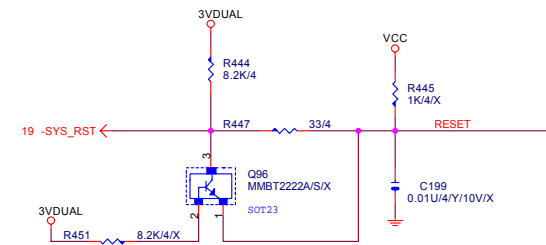
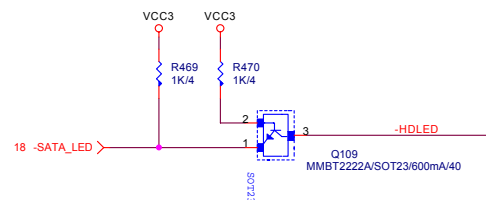
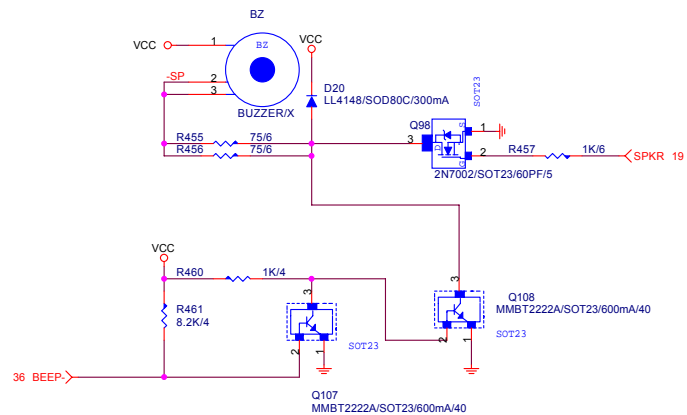
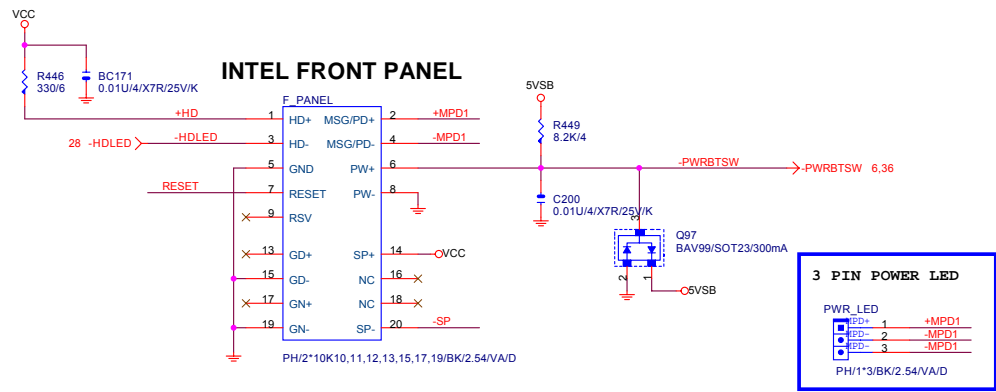
ATX POWER CONNECTOR

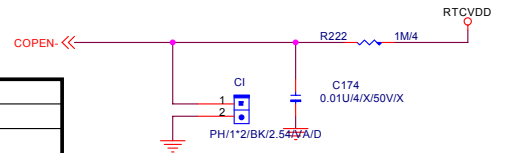
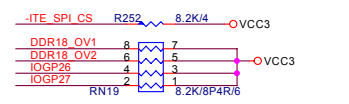
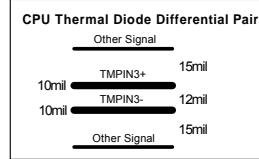
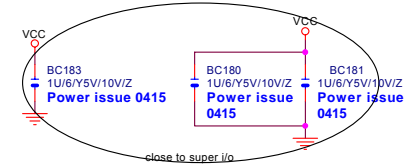
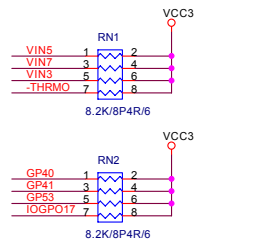
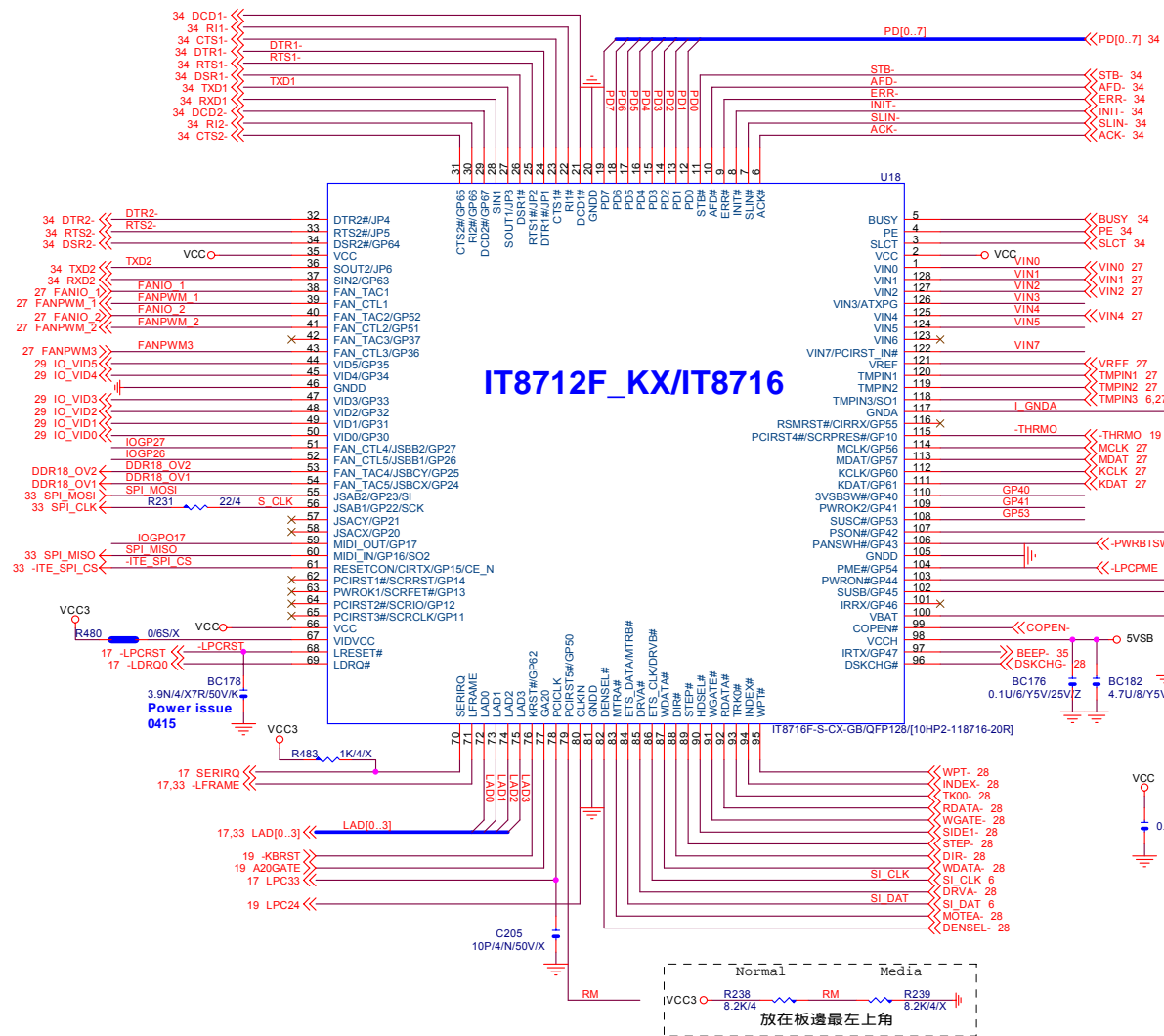


確認Ok後改為排阻







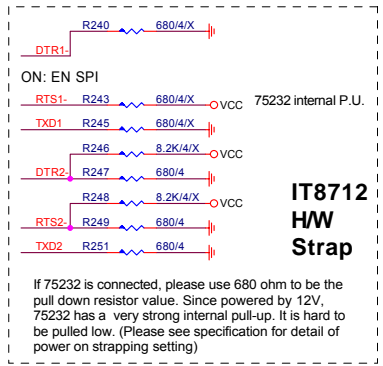


Default	Description
DTR1- 0	En SPI Flash
RTS1- 1	Midi-in/SO2 as SPI SO pin
TXD1 --	
DTR2- 0	PCIRSTx# are push-pull
RTS2- 0	Power-on FAN Duty=50%
TXD2 0	VID threshold is 0.8V/0.4V

Power On Strapping Options

Symbol	value	Description
JP1	Flashseg1_EN	Flash I/F Address Segment 1 (FFF8_0000h-FFFF_FFFFh, 000E_0000h-000F_FFFFh) is enabled
JP2	SerFlh_SO_SEL	FLH_SO2 is selected as the Serial Flash I/F SO pin. FLH_SO1 is selected as the Serial Flash I/F SO pin.
JP3	CHIP_SEL	Chip selection in configuration.
JP4	BUF_SEL	The output buffers of PCIRST1#, PCIRST2#, PCIRST3#, PCIRST4# and PCIRST5# are enhanced open-drain. It drives high about 10-20 ns when the signal transits from low to high, and then Hi-Z. The output buffers are push-pull.
JP5	FAN_CTL_SEL	The default value of EC Index 15h / 16h / 17h is 00h. The default value of EC Index 15h / 16h / 17h is 40h.
JP6	VID_SEL	The threshold voltage of VID is 2.0 / 0.8V. The threshold voltage of VID is 0.8 / 0.4V.

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